MT6761 LTE-A Smartphone Application Processor Technical Brief

Version: 1.0
Release date: 2018-05-24

Specifications are subject to change without notice.

© 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Document Revision History

Revision	Date	Author	Description
0.1	2017-11-13	SK Lee	Initial draft
0.2	2018-05-15	Shiang-Lun Kao	Updated functional block diagram.
1.0	2018-05-24	Shiang-Lun Kao	First official release.

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table of Contents

Document Revision History **2**
Table of Contents **3**
Preface **6**
1 System Overview **7**
1.1 Highlighted Features Integrated in MT6761 7
1.2 Platform Features 9
1.3 Modem Features 11
1.4 Connectivity Features 13
1.5 Multimedia Features 15
2 Product Description **17**
2.1 Pin Description 17
2.2 Electrical Characteristics 33
2.3 System Configuration 54
2.4 Power-on Sequence 55
2.5 Analog Baseband 56
2.6 Package Information 65
2.7 Power Delivery Network 66
2.8 Ordering Information 67

Lists of Figures and Tables

Figure 1-1. High-level MT6761 functional block diagram 8
Figure 2-1. Ball map view 17
Figure 2-2. LPDDR3 VIX definition 38
Figure 2-3. LPDDR3 single-ended output slew-rate definition 39
Figure 2-4. LPDDR3 differential output slew-rate definition 39
Figure 2-5. LPDDR3 RX mask 39
Figure 2-6. LPDDR4X VIX definition 40
Figure 2-7. LPDDR4X single-ended output slew-rate definition 40
Figure 2-8. LPDDR4X differential output slew-rate definition 41
Figure 2-9. LPDDR4X RX mask 41
Figure 2-10. SPI timing diagram 42
Figure 2-11. I2S master mode timing diagram 42
Figure 2-12. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz) 43
Figure 2-13. MSDC input timing diagram of default speed 44
Figure 2-14. MSDC output timing diagram of default speed 44
Figure 2-15. MSDC input timing diagram of high speed 45
Figure 2-16. MSDC output timing diagram of high speed 46
Figure 2-17. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode 46
Figure 2-18. MSDC input timing diagram of SDR50/SDR104 mode 47
Figure 2-19. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50) 47

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Figure 2-20. MSDC output timing diagram of variable window (SDR104) 47
Figure 2-21. MSDC clock timing diagram of DDR50 speed mode 48
Figure 2-22. MSDC input/output timing diagram of DDR50 speed mode 49
Figure 2-23. MSDC clock timing diagram of HS200 50
Figure 2-24. MSDC input timing diagram of HS200 50
Figure 2-25. MSDC output timing diagram of HS200 50
Figure 2-26. MSDC input timing diagram of HS400 51
Figure 2-27. MSDC output timing diagram of HS400 52
Figure 2-28. Power on sequence 55
Figure 2-29. Block diagram of BBRX-ADC 57
Figure 2-30. Block diagram of BBTX 59
Figure 2-31. Block diagram of ETDAC 60
Figure 2-32. Block diagram of DETADC 61
Figure 2-33. Block diagram of APC-DAC 62
Figure 2-34. Outlines and dimensions of VFBGA 11.4mm*11mm, 558-ball, 0.4mm pitch package 65
Figure 2-35. Top marking of MT6761 67

Table 2-1. Pin coordinate 18
Table 2-2. Acronym for pin type 21
Table 2-3. Detailed pin description 22
Table 2-4. Acronym for table of state of pins 32
Table 2-5. Absolute maximum ratings for power supply 33
Table 2-6. Recommended operating conditions for power supply 34
Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V) 35
Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V) 35
Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V) 36
Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V) 36
Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V) 36
Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V) 36
Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V) 37
Table 2-14. SIM DC electrical characteristics 37
Table 2-15. LPDDR3 AC timing parameter table of external memory interface 40
Table 2-16. LPDDR4X AC timing parameter table of external memory interface 41
Table 2-17. SPI AC timing parameters 42
Table 2-18. I2S AC timing parameters 42
Table 2-19. I2C AC timing parameters 43
Table 2-20. MSDC AC timing parameters of default speed 45
Table 2-21. MSDC AC timing parameters of high speed 46
Table 2-22. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode 47
Table 2-23. MSDC AC timing parameters of DDR50 speed mode 49
Table 2-24. MSDC AC timing parameters of HS200 51
Table 2-25. MSDC AC timing parameters of HS400 52
Table 2-26. SIM AC timing parameters 53
Table 2-27. Mode selection 54
Table 2-28. Constant tied pins 54
Table 2-29. Baseband downlink specifications 58
Table 2-30. BBTX specifications 59
Table 2-31. ETDAC specifications 60
Table 2-32. DETADC specifications 61

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 2-33. APC-DAC specifications 62
Table 2-34. AUXADC specifications 63
Table 2-35. Clock squarer specifications 64
Table 2-36. Temperature sensor specifications 64
Table 2-37. Thermal operating specifications 65
Table 2-38. PDN specifications 66

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1 System Overview

The MT6761 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A and C2K smart phone applications. The chip integrates ARM® Cortex-A53 operating up to 2.0GHz and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Quad-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

Imagination MIPS32® InterAptive, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 7, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6761 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6761 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6761

- Quad-core high performance ARM® Cortex-A53 MPCore™ operating up to 2.0GHz
- LPDDR3 up to 4GB (single channel with 32-bit data bus width)
- LPDDR4X up to 4GB (dual channels with 16-bit data bus width)
- Memory clock up to LPDDR3-1866 or LPDDR4X-3200
- LTE Cat 7 (300Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to HD+ 20:9 (1,600*720)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 21MP@30fps.
- SW dual cam 13+8MP@30fps/16+8 MP @24fps
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR, Wide-Band AMR, and EVS_WB)

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

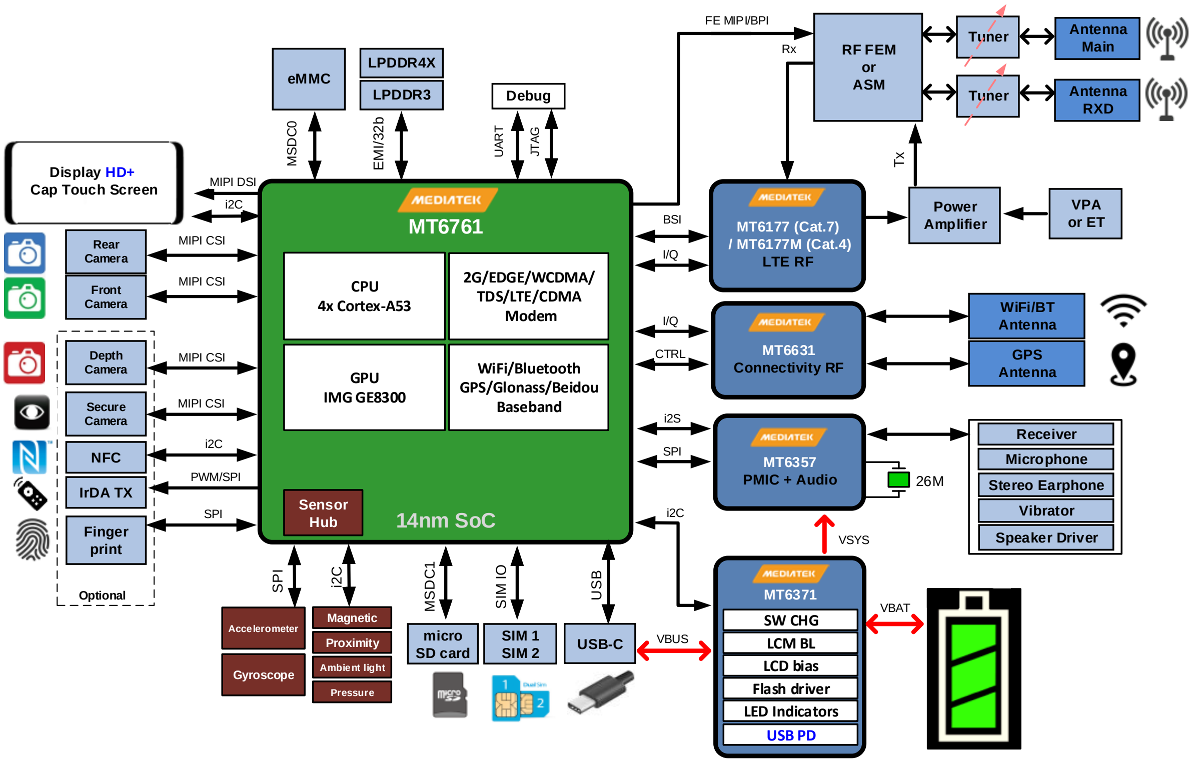


Figure 1-1. High-level MT6761 functional block diagram

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - Supports eMMC boot
  - Supports LPDDR3
  - Supports LPDDR4X

- **AP MCU subsystem**
  - Quad-core ARM® 2.0GHz Cortex-A53 MPCore™
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB L2 cache
  - DVFS technology with adaptive operating voltage from 0.65V to 1.023V

- **MD MCU subsystem**
  - Imagination MIPS32® InterAptive processor with max. 864MHz operation frequency
  - High-performance multi-core and multi-thread processor architecture (two cores and two threads)
  - 32KB L1 I-cache and 32KB L1 D-cache per core
  - 384KB SPRAM (Scratchpad memory, Two-Core's ISPRAM and DSPRAM)
  - 256KB L2 Cache (share L2 cache for two cores)
  - High-performance AXI bus Interfaces
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR3 up to 4GB (single channel with 32-bit data bus width)
  - LPDDR4X up to 4GB (dual channels with 16-bit data bus width)
  - Memory clock up to LPDDR3-1866 or LPDDR4X-3200
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 OTG mode
  - eMMC5.1
  - 2 UART for debugging and applications
  - 6 SPI masters for external devices
  - 7 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.7V/0.8V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.1V/0.6V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

- **Package**
  - Type: VFBGA
  - 11.4mm*11mm
  - Height: Max. 0.9mm
  - Ball count: 558 balls
  - Ball pitch: 0.4mm

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 300Mbps downlink, 150Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - Uplink intra-band carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - Uplink 64QAM
  - 4*2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports feICIC
  - Supports MBMS
  - Uplink CoMP ability
  - Advanced Interference Cancellation
  - Transmit Antenna Selection

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements
  - Transmit Antenna Selection

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 integrity protection
  - Transmit Antenna Selection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2, A5/3, and A5/4 ciphering
  - GPRS GEA1, GEA2, GEA3, and GEA4 ciphering
  - Programmable GSM/GPRS/EDGE modem

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

- Packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GSM circuit switch data
- GPRS/EDGE Class 12
- Supports SAIC (Single Antenna Interference Cancellation) technology
- VAMOS (Voice services over adaptive multi-user channels on one slot) technology in R9 spec
- Transmit Antenna Selection

- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Supports simultaneous hybrid dual receiver (SHDR)
  - Supports 1x/DO diversity
  - Supports SRLTE
  - Transmit antenna selection

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1.4 Connectivity Features

MT6761 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6631. With four advanced radio technologies integrated on one chip, M6763/MT6631 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)
- **Wi-Fi**
  - Dual-band (2.4/5GHz) single stream 802.11 ac/a/b/g/n MAC/BB/RF SoC, 20/40/80MHz bandwidth, MCS0~9 (256-QAM)
  - 802.11 d/e/h/i/j/k/r/v compliant
  - Security: WFA WPA/WPA2 personal, AES-CCMP, WPI-SMS4, GCMP, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports 802.11ac STBC TX/RX, 4T1R beamformee, MU-MIMO RX, WoWLAN
  - Supports MediaTek proprietary low power Green AP mode for portable hotspot operation
  - Auto rate control for optimizing the signal range and performance
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 23dBm CCK output power and 5GHz PA with max. 18.5dBm OFDM 54Mbps output power
  - RX sensitivity at 11n HT20 MCS7 mode and -62dBm 5GHz RX sensitivity at 11ac VHT80 MCS9 mode
  - Supports 32 multicast address filters and TCP/UDP/IP checksum offload
  - Per packet TX power control
- **Bluetooth**
  - Supports Bluetooth 5 dual mode for 4x the range, 2x the speed and 8x the broadcasting message capacity

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

- Integrated PA with 9dBm (class 1) transmit power or 12dBm boost mode via WIFI PA.
- RX sensitivity: GFSK -95dBm, DQPSK -94.5dBm, 8-DPSK -88dBm, BLE -98dBm
- Supports BT/Wi-Fi/LTE coexistence
- Supports 7 BT links and 16 BLE links
- Supports Packet Loss Concealment (PLC) function for better voice quality
- Supports Wideband speech
- Supports mSBC and SBC including mono and stereo
- Supports secure connection with AES128 and ECC256
- Support Adaptive Frequency Hopping with built-in channel assessment method

- **GPS**
  - Supports GPS/Glonass/Beidou/Galileo/QZSS tri-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
    - GPS/GLONASS/Beidou (G+G+B)
    - GPS/Galileo/GLONASS (G+G+G)
    - GPS/Galileo/GLONASS/Beidou (G+G+G+B)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 8dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBµVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to HD+ (1600*720)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 6 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling

- **Graphics**
  - OpenGL ES 3.1/3.0/2.0/1.1 3D graphic accelerator capable of processing 160M tri/sec and 1,600M pixel/sec @ 770MHz
  - OpenCL ES 1.1 full profile

- **Image**
  - Integrated image signal processor supports 21MP@30fps
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 21M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - Hardware JPEG encoder: Baseline encoding with 130M pixel/sec; Continuous shot with 220M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps/40Mbps
  - VP9 decoder 1080p @ 30fps/40Mbps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG2 decoder 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps
  - H.263 encoder: Simple profile D1 @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM
  - External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
  - 4-band IIR compensation filter to enhance loudspeaker responses

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

- Proprietary audio post-processing technologies: BesLoudness (MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR, Wide-Band AMR, and EVS_WB)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o wind noise rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

558	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	NC	WF_IN	WF_IP		EMI0_CA9		NC		EMI0_CS0_N		DVSS		DVSS		DVSS		EMI0_DQ8		EMI0_DQ15		EMI0_DQ31		MSDC0_DAT4		MSDC0_DAT2	MSDC0_DAT7	DVDD18_MSDC0	NC	A
B	WF_QP	WF_QN	DVSS	EMI_EXTR	EMI0_CA4		EMI0_CA1	EMI0_CA0	NC		EMI0_DQ21	EMI0_DQ22	EMI0_DQ20		EMI0_DQ4	EMI0_DM0	EMI0_DQ7		EMI0_DM3	EMI0_DQ28	DVSS		MSDC0_DAT5	MSDC0_DAT6	MSDC0_CMD	MSDC0_DSL	USB_DM	AVDD33_USB	B
C		DVSS	AVDD12_WBG	NC	EMI0_CA6	DVSS	EMI0_CA2		NC	EMI0_DQ18	EMI0_DQ17	DVSS	EMI0_DQ0	EMI0_DQ2	EMI0_DQ1	DVSS	EMI0_DM1	EMI0_DQ11	EMI0_DQ14	DVSS	EMI0_DQ30	EMI0_DQ29	DVSS	MSDC0_DAT3	MSDC0_RSTB	MSDC0_DAT0	USB_DP		C
D	BT_IN	BT_IP	DVSS	NC	EMI0_CA5	EMI0_CA3	NC	EMI0_CKE0	DVSS	EMI0_DQ16	NC	EMI0_DQ19	DVSS	EMI0_DQS0_T	EMI0_DQ5		EMI0_DQS1_C	NC	EMI0_DQ12	EMI0_DQ24	EMI0_DQ27	EMI0_DQS3_T	DVSS	MSDC0_DAT1	MSDC0_CLK	CHD_DP	DVSS	AVDD18_USB	D
E			BT_QP	DVSS	EMI0_CA8	EMI0_CA7	EMI0_CKE1	EMI0_CS1_N	EMI0_CK_C	EMI0_DM2	EMI0_DQ23		EMI0_DQS2_C	EMI0_DQS0_C	EMI0_DQ3	EMI0_DQ6	EMI0_DQS1_T	EMI0_DQ9	EMI0_DQ13	EMI0_DQ25	EMI0_DQ26	EMI0_DQS3_C	NC	DVSS	DVSS	CHD_DM	SYSRSTB	AVDD12_USB	E
F	GPS_I	DVSS	BT_QN	DVSS	DVSS	DVSS	DVSS	DVSS	EMI0_CK_T	DVSS	DVSS	DVSS	EMI0_DQS2_T	DVSS		VREF_EMI	DVSS	EMI0_DQ10	DVSS	DVSS	DVSS	DVSS	DVSS	GPIO_EXT2	GPIO_EXT1	GPIO_EXT4	TESTMODE		F
G	GPS_Q	CONN_WB_PTA	CONN_HRST_B	DVSS		DVSS	XIN_WBG				DVSS	DVSS	DVSS	DVSS	DVSS	NC					DVSS	DVSS	GPIO_EXT0	GPIO_EXT3	GPIO_EXT5	DVSS	AUD_CLK_MISO	DVDD18_IOLT	G
H		AVDD18_WBG	CONN_WF_CTRL2	CONN_WF_CTRL1	CONN_WF_CTRL0					AVDD2_EMI	AVDDQ_EMI0	AVDDQ_EMI0	AVDD2_EMI	DVSS	DVSS		AVDD2_EMI	AVDDQ_EMI1	AVDDQ_EMI1	AVDD2_EMI	AVDD18_DDR	DVSS	GPIO_EXT6	GPIO_EXT7	DVSS	RTC32K_CK	AUD_SYNC_MISO		H
J	DVDD18_IORT	CAM_CLK2	SCL6	SDA6	CONN_BT_CLK	CONN_TOP_CLK															DVDD_TOP	DVSS	DVSS	DVSS	AUD_CLK_MOSI	AUD_SYNC_MOSI	AUD_DAT_MISO0	AUD_DAT_MISO1	J
K		CAM_PDN2	CAM_RST2	ANT_SEL2	ANT_SEL0	ANT_SEL1	CONN_TOP_DATA	CONN_BT_DATA	DVSS	DVDD_TOP	DVSS	DVSS	DVDD_TOP	DVDD_TOP	DVSS	DVSS	DVDD_TOP	DVSS		DVDD_MFGSYS				WATCHDOG	AUD_DAT_MOSI1	AUD_DAT_MOSI0	PWRAP_SPI0_CSN	PWRAP_SPI0_MI	K
L	CSI1A_L1P	CSI1A_L1N	CSI1A_L0P	CSI1A_L0N	CSI1B_L0P			DVSS			DVSS		DVDD_TOP_SRAM		DVSS	DVSS	DVDD_TOP		DVDD_MFGSYS	DVDD_MFGSYS	DVSS	DVSS		CAM_PDN3	SRCLKENA0	DVSS	PWRAP_SPI0_CK		L
M	CSI1A_L2P	CSI1A_L2N	CSI1B_L1P	CSI1B_L1N	CSI1B_L0N	DVSS	DVSS			DVDD_TOP		DVSS		DVDD_TOP		DVSS		DVDD_TOP		DVDD_MFGSYS		DVSS		DVSS	SRCLKENA1	EINT12	PWRAP_SPI0_MO	DVSS	M
N	CSI0A_L1P	CSI0A_L1N	CSI0A_L0P	CSI0A_L0N	CSI0B_L2P	DVSS	DVSS				DVSS		DVDD_TOP		DVSS		DVDD_TOP		DVDD_MFGSYS	DVDD_MFGSYS	DVSS	DVSS			DSI0_D0P	DSI0_D0N	DSI0_D1N	DSI0_D1P	N
P	CSI0A_L2P	CSI0A_L2N	CSI0B_L0P	CSI0B_L0N	CSI0B_L2N		DVSS			DVDD_TOP		DVSS	DVDD_TOP	DVDD_TOP		DVSS		DVDD_TOP		DVDD_MFGSYS	DVSS	DVSS	DVDD_TOP		DSI0_CKP	DSI0_CKN	DSI0_D3P		P
R	CSI2A_L0P	CSI2A_L0N	CSI0B_L1P	CSI0B_L1N	CSI2B_L1P				DVDD_VDD_MODE		DVSS		DVDD_TOP		DVSS		DVDD_TOP		DVDD_MFG_SRAM		DVSS	DVSS			DSI0_D2P	DSI0_D2N	DSI0_D3N	AVDD12_DSI	R
T	CSI2A_L1P	CSI2A_L1N	CSI2A_L2P	CSI2A_L2N	CSI2B_L1N			DVSS		DVDD_VDD_MODE		DVSS		AVDD12_PLLGP		AVDD18_PLLGP		DVDD_TOP		DVDD_MFGSYS	DVDD_MFGSYS	DVSS		SPI2_CLK	SPI2_MO	SPI2_CSB	SPI4_MO	AVDD04_DSI	T
U	DVDD18_IORB	AVDD12_CSI	CSI2B_L0P	CSI2B_L0N		SCL4			DVDD_VDD_MODE		DVSS		DVDD_VDD_MODE			DVDD_DVFS		DVDD_DVFS		DVDD_DVFS		DVDD_DVFS	SPI1_CSB	SPI2_MI	SPI3_MI	SPI3_CSB	SPI4_MI		U
V	CAM_RST1	CAM_RST0	SDA2	SCL2		SDA4		DVSS		DVDD_VDD_MODE		DVDD_TOP_SRAM	DVDD_VDD_MODE		DVDD_MCUSYS_SRA	DVSS	DVSS		DVSS		DVSS			SPI1_CLK	SPI3_CLK	SPI3_MO	SPI4_CLK	SPI4_CSB	V
W		CAM_CLK1	EINT10	EINT9	CAM_CLK0	CAM_PDN0	EINT11	DVDD_VDD_MODE	DVDD_VDD_MODE	DVDD_VDD_MODE		TN_PLLGP	TP_PLLGP				DVSS		DVSS		DVSS			SPI1_MI	MSDC1_DAT3	MSDC1_CLK	MSDC1_CMD	DVDD18_IOLM	W
Y	SRCLKENAI	CAM_PDN1	EINT7	EINT6		EINT4	EINT5	DVDD_VDD_MODE								DVDD_DVFS		DVDD_DVFS		DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	GPIO_EXT9	SPI1_MO	SIM1_SIO	MSDC1_DAT1	MSDC1_DAT0		Y
AA	KPROW0	UTXD0	URXD0	EINT3	EINT2	EINT8	EINT1		DVSS		DVSS		DVSS			DVDD_DVFS		DVDD_DVFS		DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	GPIO_EXT10	GPIO_EXT8	SIM1_SCLK	SIM1_SRST	MSDC1_DAT2	DVDD18_MSDC1	AA
AB	KPROW1	KPCOL1	KPCOL0	EINT0	SCL0	CDM5P5A				DVSS		DVSS	MAIN_X26M_IN			DVDD_DVFS		DVDD_DVFS					SCL5		SIM2_SIO	DRVBUS	IDDIG	DVDD18_SIM	AB
AC	SPI0_CSB	SPI0_MO	PWM0	SDA0	CDM3P5A	BPI_BUS7			RFIC_ET0_N	APC								AVDD18_CPU	GPIO_EXT15	GPIO_EXT14	SCL3	SDA3	SDA5	PERIPHERAL_EN3	SIM2_SCLK	SIM2_SRST		DVDD28_SIM2	AC
AD	SPI0_MI	SPI0_CLK	BPI_PA_VM0	BPI_BUS11_OLAT0	MISC_BSI_DO3	MISC_BSI_DO2	DVSS	RFIC_ET0_P	TX_BB_IN0	TX_BB_QN0	DVSS	DRX_BB_Q0P	DRX_BB_I0P	DVSS				DVDD_VQPS	GPIO_EXT13	GPIO_EXT12	GPIO_EXT11	PERIPHERAL_EN0	PERIPHERAL_EN2	PERIPHERAL_EN1	BPI_BUS8	LCM_RST	DISP_PWM	DVDD28_MSDC1	AD
AE	SCL1	BPI_PA_VM1	BPI_BUS14_ANT1	BPI_BUS0	MISC_BSI_CK3	MISC_BSI_CK2		DVSS	TX_BB_IP0	TX_BB_QP0	DVSS	DRX_BB_Q0N	DRX_BB_I0N	DVSS			AUXIN4	AUXIN3	AUXIN2	RFIC0_BSI_D0	RFIC0_BSI_EN	PERIPHERAL_EN5	PERIPHERAL_EN4	BPI_BUS12_OLAT1	BPI_BUS13_ANT0	INT_SIM1	DSI_TE	DVDD28_SIM1	AE
AF	SDA1	BPI_BUS1	BPI_BUS2	BPI_BUS3	MISC_BSI_CK1	MISC_BSI_DO1	MISC_BSI_DO0	DVSS	DET_IN0	DET_QP0	DVSS	PRX_BB_Q0P	PRX_BB_I0P	DVSS	PRX_BB_I1	DRX_BB_Q1	DVSS	REFP	AUXIN1	AUXIN0	RFIC0_BSI_D1	RFIC0_BSI_CK	CAM_RST3	BPI_BUS15_ANT2	BPI_BUS10	BPI_BUS9	INT_SIM2	DVSS	AF
AG	NC	BPI_BUS4	BPI_BUS5	BPI_BUS6		DVDD18_IORB	MISC_BSI_CK0		DET_IP0	DET_QN0		PRX_BB_Q0N	PRX_BB_I0N		PRX_BB_Q1	DRX_BB_I1		AVDD18_AP	AVDD18_MD		AVDD12_MD	RFIC0_BSI_D2		CAM_CLK3		DVSS	DVDD18_IOBL	NC	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

Figure 2-1. Ball map view

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	J3	SCL6	W5	CAM_CLK0
A2	WF_IN	J4	SDA6	W6	CAM_PDN0
A3	WF_IP	J5	CONN_BT_CLK	W7	EINT11
A5	EMI0_CA9	J6	CONN_TOP_CLK	W8	DVDD_VDD_MODEM
A7	N	J21	DVDD_TOP	W9	DVDD_VDD_MODEM
A9	EMI0_CS0_N	J22	DVSS	W10	DVDD_VDD_MODEM
A11	DVSS	J23	DVSS	W12	TN_PLLGP
A13	DVSS	J24	DVSS	W13	TP_PLLGP
A15	DVSS	J25	AUD_CLK_MOSI	W17	DVSS
A17	EMI0_DQ8	J26	AUD_SYNC_MOSI	W19	DVSS
A19	EMI0_DQ15	J27	AUD_DAT_MISO0	W21	DVSS
A21	EMI0_DQ31	J28	AUD_DAT_MISO1	W24	SPI1_MI
A23	MSDC0_DAT4	K2	CAM_PDN2	W25	MSDC1_DAT3
A25	MSDC0_DAT2	K3	CAM_RST2	W26	MSDC1_CLK
A26	MSDC0_DAT7	K4	ANT_SEL2	W27	MSDC1_CMD
A27	DVDD18_MSDC0	K5	ANT_SEL0	W28	DVDD18_IOLM
A28	NC	K6	ANT_SEL1	Y1	SRCLKENAI
B1	WF_QP	K7	CONN_TOP_DATA	Y2	CAM_PDN1
B2	WF_QN	K8	CONN_BT_DATA	Y3	EINT7
B3	DVSS	K9	DVSS	Y4	EINT6
B4	EMI_EXTR	K10	DVDD_TOP	Y6	EINT4
B5	EMI0_CA4	K11	DVSS	Y7	EINT5
B7	EMI0_CA1	K12	DVSS	Y8	DVDD_VDD_MODEM
B8	EMI0_CA0	K13	DVDD_TOP	Y16	DVDD_DVFS
B9	N	K14	DVDD_TOP	Y18	DVDD_DVFS
B11	EMI0_DQ21	K15	DVSS	Y20	DVDD_DVFS
B12	EMI0_DQ22	K16	DVSS	Y21	DVDD_DVFS
B13	EMI0_DQ20	K17	DVDD_TOP	Y22	DVDD_DVFS
B15	EMI0_DQ4	K18	DVSS	Y23	GPIO_EXT9
B16	EMI0_DM0	K20	DVDD_MFGSYS	Y24	SPI1_MO
B17	EMI0_DQ7	K24	WATCHDOG	Y25	SIM1_SIO
B19	EMI0_DM3	K25	AUD_DAT_MOSI1	Y26	MSDC1_DAT1
B20	EMI0_DQ28	K26	AUD_DAT_MOSI0	Y27	MSDC1_DAT0
B21	DVSS	K27	PWRAP_SPI0_CSN	AA1	KPROW0
B23	MSDC0_DAT5	K28	PWRAP_SPI0_MI	AA2	UTXD0
B24	MSDC0_DAT6	L1	CSI1A_L1P	AA3	URXD0
B25	MSDC0_CMD	L2	CSI1A_L1N	AA4	EINT3
B26	MSDC0_DSL	L3	CSI1A_L0P	AA5	EINT2
B27	USB_DM	L4	CSI1A_L0N	AA6	EINT8
B28	AVDD33_USB	L5	CSI1B_L0P	AA7	EINT1
C2	DVSS	L8	DVSS	AA9	DVSS
C3	AVDD12_WBG	L11	DVSS	AA11	DVSS
C4	N	L13	DVDD_TOP_SRAM	AA13	DVSS
C5	EMI0_CA6	L15	DVSS	AA16	DVDD_DVFS
C6	DVSS	L16	DVSS	AA18	DVDD_DVFS
C7	EMI0_CA2	L17	DVDD_TOP	AA20	DVDD_DVFS
C9	N	L19	DVDD_MFGSYS	AA21	DVDD_DVFS

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C10	EMI0_DQ18	L20	DVDD_MFGSYS	AA22	DVDD_DVFS
C11	EMI0_DQ17	L21	DVSS	AA23	GPIO_EXT10
C12	DVSS	L22	DVSS	AA24	GPIO_EXT8
C13	EMI0_DQ0	L24	CAM_PDN3	AA25	SIM1_SCLK
C14	EMI0_DQ2	L25	SRCLKENA0	AA26	SIM1_SRST
C15	EMI0_DQ1	L26	DVSS	AA27	MSDC1_DAT2
C16	DVSS	L27	PWRAP_SPI0_CK	AA28	DVDD18_MSDC1
C17	EMI0_DM1	M1	CSI1A_L2P	AB1	KPROW1
C18	EMI0_DQ11	M2	CSI1A_L2N	AB2	KPCOL1
C19	EMI0_DQ14	M3	CSI1B_L1P	AB3	KPCOL0
C20	DVSS	M4	CSI1B_L1N	AB4	EINT0
C21	EMI0_DQ30	M5	CSI1B_L0N	AB5	SCL0
C22	EMI0_DQ29	M6	DVSS	AB6	CDM5P5A
C23	DVSS	M7	DVSS	AB10	DVSS
C24	MSDC0_DAT3	M10	DVDD_TOP	AB12	DVSS
C25	MSDC0_RSTB	M12	DVSS	AB13	MAIN_X26M_IN
C26	MSDC0_DAT0	M14	DVDD_TOP	AB16	DVDD_DVFS
C27	USB_DP	M16	DVSS	AB18	DVDD_DVFS
D1	BT_IN	M18	DVDD_TOP	AB23	SCL5
D2	BT_IP	M20	DVDD_MFGSYS	AB25	SIM2_SIO
D3	DVSS	M22	DVSS	AB26	DRVBUS
D4	N	M24	DVSS	AB27	IDDIG
D5	EMI0_CA5	M25	SRCLKENA1	AB28	DVDD18_SIM
D6	EMI0_CA3	M26	EINT12	AC1	SPI0_CSB
D7	N	M27	PWRAP_SPI0_MO	AC2	SPI0_MO
D8	EMI0_CKE0	M28	DVSS	AC3	PWM0
D9	DVSS	N1	CSI0A_L1P	AC4	SDA0
D10	EMI0_DQ16	N2	CSI0A_L1N	AC5	CDM3P5A
D11	N	N3	CSI0A_L0P	AC6	BPI_BUS7
D12	EMI0_DQ19	N4	CSI0A_L0N	AC9	RFIC_ET0_N
D13	DVSS	N5	CSI0B_L2P	AC10	APC
D14	EMI0_DQS0_T	N6	DVSS	AC18	AVDD18_CPU
D15	EMI0_DQ5	N7	DVSS	AC19	GPIO_EXT15
D17	EMI0_DQS1_C	N11	DVSS	AC20	GPIO_EXT14
D18	N	N13	DVDD_TOP	AC21	SCL3
D19	EMI0_DQ12	N15	DVSS	AC22	SDA3
D20	EMI0_DQ24	N17	DVDD_TOP	AC23	SDA5
D21	EMI0_DQ27	N19	DVDD_MFGSYS	AC24	PERIPHERAL_EN3
D22	EMI0_DQS3_T	N20	DVDD_MFGSYS	AC25	SIM2_SCLK
D23	DVSS	N21	DVSS	AC26	SIM2_SRST
D24	MSDC0_DAT1	N22	DVSS	AC28	DVDD28_SIM2
D25	MSDC0_CLK	N25	DSI0_D0P	AD1	SPI0_MI
D26	CHD_DP	N26	DSI0_D0N	AD2	SPI0_CLK
D27	DVSS	N27	DSI0_D1N	AD3	BPI_PA_VM0
D28	AVDD18_USB	N28	DSI0_D1P	AD4	BPI_BUS11_OLAT0
E3	BT_QP	P1	CSI0A_L2P	AD5	MISC_BSI_DO_3
E4	DVSS	P2	CSI0A_L2N	AD6	MISC_BSI_DO_2
E5	EMI0_CA8	P3	CSI0B_L0P	AD7	DVSS
E6	EMI0_CA7	P4	CSI0B_L0N	AD8	RFIC_ET0_P
E7	EMI0_CKE1	P5	CSI0B_L2N	AD9	TX_BB_IN0
E8	EMI0_CS1_N	P7	DVSS	AD10	TX_BB_QN0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
E9	EMI0_CK_C	P10	DVDD_TOP	AD11	DVSS
E10	EMI0_DM2	P12	DVSS	AD12	DRX_BB_Q0P
E11	EMI0_DQ23	P13	DVDD_TOP	AD13	DRX_BB_I0P
E13	EMI0_DQS2_C	P14	DVDD_TOP	AD14	DVSS
E14	EMI0_DQS0_C	P16	DVSS	AD18	DVDD_VQPS
E15	EMI0_DQ3	P18	DVDD_TOP	AD19	GPIO_EXT13
E16	EMI0_DQ6	P20	DVDD_MFGSYS	AD20	GPIO_EXT12
E17	EMI0_DQS1_T	P21	DVSS	AD21	GPIO_EXT11
E18	EMI0_DQ9	P22	DVSS	AD22	PERIPHERAL_EN0
E19	EMI0_DQ13	P23	DVDD_TOP	AD23	PERIPHERAL_EN2
E20	EMI0_DQ25	P25	DSI0_CKP	AD24	PERIPHERAL_EN1
E21	EMI0_DQ26	P26	DSI0_CKN	AD25	BPI_BUS8
E22	EMI0_DQS3_C	P27	DSI0_D3P	AD26	LCM_RST
E23	N	R1	CSI2A_L0P	AD27	DISP_PWM
E24	DVSS	R2	CSI2A_L0N	AD28	DVDD28_MSDC1
E25	DVSS	R3	CSI0B_L1P	AE1	SCL1
E26	CHD_DM	R4	CSI0B_L1N	AE2	BPI_PA_VM1
E27	SYSRSTB	R5	CSI2B_L1P	AE3	BPI_BUS14_ANT1
E28	AVDD12_USB	R9	DVDD_VDD_MODEM	AE4	BPI_BUS0
F1	GPS_I	R11	DVSS	AE5	MISC_BSI_CK_3
F2	DVSS	R13	DVDD_TOP	AE6	MISC_BSI_CK_2
F3	BT_QN	R15	DVSS	AE8	DVSS
F4	DVSS	R17	DVDD_TOP	AE9	TX_BB_IP0
F5	DVSS	R19	DVDD_MFG_SRAM	AE10	TX_BB_QP0
F6	DVSS	R21	DVSS	AE11	DVSS
F7	DVSS	R22	DVSS	AE12	DRX_BB_Q0N
F8	DVSS	R25	DSI0_D2P	AE13	DRX_BB_I0N
F9	EMI0_CK_T	R26	DSI0_D2N	AE14	DVSS
F10	DVSS	R27	DSI0_D3N	AE17	AUXIN4
F11	DVSS	R28	AVDD12_DSI	AE18	AUXIN3
F12	DVSS	T1	CSI2A_L1P	AE19	AUXIN2
F13	EMI0_DQS2_T	T2	CSI2A_L1N	AE20	RFIC0_BSI_D0
F14	DVSS	T3	CSI2A_L2P	AE21	RFIC0_BSI_EN
F16	VREF_EMI	T4	CSI2A_L2N	AE22	PERIPHERAL_EN5
F17	DVSS	T5	CSI2B_L1N	AE23	PERIPHERAL_EN4
F18	EMI0_DQ10	T8	DVSS	AE24	BPI_BUS12_OLAT1
F19	DVSS	T10	DVDD_VDD_MODEM	AE25	BPI_BUS13_ANT0
F20	DVSS	T12	DVSS	AE26	INT_SIM1
F21	DVSS	T14	AVDD12_PLLGP	AE27	DSI_TE
F22	DVSS	T16	AVDD18_PLLGP	AE28	DVDD28_SIM1
F23	DVSS	T18	DVDD_TOP	AF1	SDA1
F24	GPIO_EXT2	T20	DVDD_MFGSYS	AF2	BPI_BUS1
F25	GPIO_EXT1	T21	DVDD_MFGSYS	AF3	BPI_BUS2
F26	GPIO_EXT4	T22	DVSS	AF4	BPI_BUS3
F27	TESTMODE	T24	SPI2_CLK	AF5	MISC_BSI_CK_1
G1	GPS_Q	T25	SPI2_MO	AF6	MISC_BSI_DO_1
G2	CONN_WB_PTA	T26	SPI2_CSB	AF7	MISC_BSI_DO_0
G3	CONN_HRST_B	T27	SPI4_MO	AF8	DVSS
G4	DVSS	T28	AVDD04_DSI	AF9	DET_IN0
G6	DVSS	U1	DVDD18_IORB	AF10	DET_QP0
G7	XIN_WBG	U2	AVDD12_CSI	AF11	DVSS

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
G11	DVSS	U3	CSI2B_L0P	AF12	PRX_BB_Q0P
G12	DVSS	U4	CSI2B_L0N	AF13	PRX_BB_I0P
G13	DVSS	U6	SCL4	AF14	DVSS
G14	DVSS	U9	DVDD_VDD_MODEM	AF15	PRX_BB_I1
G15	DVSS	U11	DVSS	AF16	DRX_BB_Q1
G16	N	U13	DVDD_VDD_MODEM	AF17	DVSS
G21	DVSS	U16	DVDD_DVFS	AF18	REFP
G22	DVSS	U18	DVDD_DVFS	AF19	AUXIN1
G23	GPIO_EXT0	U20	DVDD_DVFS	AF20	AUXIN0
G24	GPIO_EXT3	U22	DVDD_DVFS	AF21	RFIC0_BSI_D1
G25	GPIO_EXT5	U23	SPI1_CSB	AF22	RFIC0_BSI_CK
G26	DVSS	U24	SPI2_MI	AF23	CAM_RST3
G27	AUD_CLK_MISO	U25	SPI3_MI	AF24	BPI_BUS15_ANT2
G28	DVDD18_IOLT	U26	SPI3_CSB	AF25	BPI_BUS10
H2	AVDD18_WBG	U27	SPI4_MI	AF26	BPI_BUS9
H3	CONN_WF_CTRL2	V1	CAM_RST1	AF27	INT_SIM2
H4	CONN_WF_CTRL1	V2	CAM_RST0	AF28	DVSS
H5	CONN_WF_CTRL0	V3	SDA2	AG1	NC
H10	AVDD2_EMI	V4	SCL2	AG2	BPI_BUS4
H11	AVDDQ_EMI0	V6	SDA4	AG3	BPI_BUS5
H12	AVDDQ_EMI0	V8	DVSS	AG4	BPI_BUS6
H13	AVDD2_EMI	V10	DVDD_VDD_MODEM	AG6	DVDD18_IORB
H14	DVSS	V12	DVDD_TOP_SRAM	AG7	MISC_BSI_CK_0
H15	DVSS	V13	DVDD_VDD_MODEM	AG9	DET_IP0
H17	AVDD2_EMI	V15	DVDD_MCUSYS_SRAM	AG10	DET_QN0
H18	AVDDQ_EMI1	V16	DVSS	AG12	PRX_BB_Q0N
H19	AVDDQ_EMI1	V17	DVSS	AG13	PRX_BB_I0N
H20	AVDD2_EMI	V19	DVSS	AG15	PRX_BB_Q1
H21	AVDD18_DDR	V21	DVSS	AG16	DRX_BB_I1
H22	DVSS	V24	SPI1_CLK	AG18	AVDD18_AP
H23	GPIO_EXT6	V25	SPI3_CLK	AG19	AVDD18_MD
H24	GPIO_EXT7	V26	SPI3_MO	AG21	AVDD12_MD
H25	DVSS	V27	SPI4_CLK	AG22	RFIC0_BSI_D2
H26	RTC32K_CK	V28	SPI4_CSB	AG24	CAM_CLK3
H27	AUD_SYNC_MISO	W2	CAM_CLK1	AG26	DVSS
J1	DVDD18_IORT	W3	EINT10	AG27	DVDD18_IOBL
J2	CAM_CLK2	W4	EINT9	AG28	NC

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Abbreviation	Description
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-3. Detailed pin description

Pin name	Pin no.	Type	Description	Power domain
SYSTEM				
SYSRSTB	E27	DI	System reset input	DVDD18
WATCHDOG	K24	DIO	Watchdog reset output	DVDD18
TESTMODE	F27	DI	Test mode	DVDD18
RTC32K_CK	H26	DIO	RTC 32K input	DVDD18
SRCLKENA0	L25	DIO	Output signal; control 26Hz/Buck/LDO normal mode or sleep mode. (High: normal mode; low: sleep mode or low power mode)	DVDD18
SRCLKENA1	M25	DIO	Output signal; control VRF18. (High: VRF18 on; low: VRF18 off)	DVDD18
SRCLKENAI	Y1	DIO	Input signal; NFC 26MHz request signal. (High: NFC chip requests system to provide 26MHz to NFC chip)	DVDD18
EINT0	AB4	DIO	External interrupt input	DVDD18
EINT1	AA7	DIO	External interrupt input	DVDD18
EINT2	AA5	DIO	External interrupt input	DVDD18
EINT3	AA4	DIO	External interrupt input	DVDD18
EINT4	Y6	DIO	External interrupt input	DVDD18
EINT5	Y7	DIO	External interrupt input	DVDD18
EINT6	Y4	DIO	External interrupt input	DVDD18
EINT7	Y3	DIO	External interrupt input	DVDD18
EINT8	AA6	DIO	External interrupt input	DVDD18
EINT9	W4	DIO	External interrupt input	DVDD18
EINT10	W3	DIO	External interrupt input	DVDD18
EINT11	W7	DIO	External interrupt input	DVDD18
EINT12	M26	DIO	External interrupt input	DVDD18
GPIOs				
GPIO_EXT0	G23	DI	General purpose input or output pin	DVDD18
GPIO_EXT1	F25	DIO	General purpose input or output pin	DVDD18
GPIO_EXT2	F24	DI	General purpose input or output pin	DVDD18
GPIO_EXT3	G24	DIO	General purpose input or output pin	DVDD18
GPIO_EXT4	F26	DIO	General purpose input or output pin	DVDD18
GPIO_EXT5	G25	DIO	General purpose input or output pin	DVDD18
GPIO_EXT6	H23	DIO	General purpose input or output pin	DVDD18
GPIO_EXT7	H24	DIO	General purpose input or output pin	DVDD18

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
GPIO_EXT8	AA24	DIO	General purpose input or output pin	DVDD18
GPIO_EXT9	Y23	DIO	General purpose input or output pin	DVDD18
GPIO_EXT10	AA23	DIO	General purpose input or output pin	DVDD18
GPIO_EXT11	AD21	DIO	General purpose input or output pin	DVDD18
GPIO_EXT12	AD20	DIO	General purpose input or output pin	DVDD18
GPIO_EXT13	AD19	DIO	General purpose input or output pin	DVDD18
GPIO_EXT14	AC20	DIO	General purpose input or output pin	DVDD18
GPIO_EXT15	AC19	DIO	General purpose input or output pin	DVDD18
PERIPHERAL_EN0	AD22	DIO	Peripheral enable output pin	DVDD18
PERIPHERAL_EN1	AD24	DIO	Peripheral enable output pin	DVDD18
PERIPHERAL_EN2	AD23	DIO	Peripheral enable output pin	DVDD18
PERIPHERAL_EN3	AC24	DIO	Peripheral enable output pin	DVDD18
PERIPHERAL_EN4	AE23	DIO	Peripheral enable output pin	DVDD18
PERIPHERAL_EN5	AE22	DIO	Peripheral enable output pin	DVDD18
PMIC				
PWRAP_SPI0_MO	M27	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_MI	K28	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CSN	K27	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CK	L27	DIO	PMIC SPI control interface	DVDD18
AUD_CLK_MOSI	J25	DIO	PMIC audio input interface	DVDD18
AUD_CLK_MISO	G27	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MISO	H27	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MOSI	J26	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO0	J27	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO1	J28	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI0	K26	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI1	K25	DIO	PMIC audio input interface	DVDD18
SIM				
SIM1_SCLK	AA25	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	Y25	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	AA26	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	AC25	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	AB25	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	AC26	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	AE26	DIO	SIM1 interrupt	DVDD18
INT_SIM2	AF27	DIO	SIM2 interrupt	DVDD18
LCD				
DSI_TE	AE27	DIO	Parallel display interface tearing effect	DVDD18
LCM_RST	AD26	DIO	Parallel display interface reset signal	DVDD18
PWM				
PWM0	AC3	DIO	PWM0	DVDD18

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
DISP_PWM	AD27	DIO	Display PWM	DVDD18
Keypad Interface				
KPCOL0	AB3	DIO	Keypad column 0	DVDD18
KPCOL1	AB2	DIO	Keypad column 1	DVDD18
KPROW0	AA1	DIO	Keypad row 0	DVDD18
KPROW1	AB1	DIO	Keypad row 1	DVDD18
SPI				
SPI0_CSB	AC1	DIO	SPI0 chip select	DVDD18
SPI0_MI	AD1	DIO	SPI0 data in	DVDD18
SPI0_MO	AC2	DIO	SPI0 data out	DVDD18
SPI0_CLK	AD2	DIO	SPI0 clock	DVDD18
SPI1_CSB	U23	DIO	SPI1 chip select	DVDD18
SPI1_MI	W24	DIO	SPI1 data in	DVDD18
SPI1_MO	Y24	DIO	SPI1 data out	DVDD18
SPI1_CLK	V24	DIO	SPI1 clock	DVDD18
SPI2_CSB	T26	DIO	SPI2 chip select	DVDD18
SPI2_MI	U24	DIO	SPI2 data in	DVDD18
SPI2_MO	T25	DIO	SPI2 data out	DVDD18
SPI2_CLK	T24	DIO	SPI clock	DVDD18
SPI3_CSB	U26	DIO	SPI3 chip select	DVDD18
SPI3_MI	U25	DIO	SPI3 data in	DVDD18
SPI3_MO	V26	DIO	SPI3 data out	DVDD18
SPI3_CLK	V25	DIO	SPI3 clock	DVDD18
SPI4_CSB	V28	DIO	SPI4 chip select	DVDD18
SPI4_MI	U27	DIO	SPI4 data in	DVDD18
SPI4_MO	T27	DIO	SPI4 data out	DVDD18
SPI4_CLK	V27	DIO	SPI4 clock	DVDD18
UR				
UTXD0	AA2	DIO	UR interdace	DVDD18
URXD0	AA3	DIO	SPI data in	DVDD18
BPI				
BPI_BUS0	AE4	DIO	BPI_BUS0	DVDD18
BPI_BUS1	AF2	DIO	BPI_BUS1	DVDD18
BPI_BUS2	AF3	DIO	BPI_BUS2	DVDD18
BPI_BUS3	AF4	DIO	BPI_BUS3	DVDD18
BPI_BUS4	AG2	DIO	BPI_BUS4	DVDD18
BPI_BUS5	AG3	DIO	BPI_BUS5	DVDD18
BPI_BUS6	AG4	DIO	BPI_BUS6	DVDD18
BPI_BUS7	AC6	DIO	BPI_BUS7	DVDD18
BPI_BUS8	AD25	DIO	BPI_BUS8	DVDD18
BPI_BUS9	AF26	DIO	BPI_BUS9	DVDD18

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
BPI_BUS10	AF25	DIO	BPI_BUS10	DVDD18
BPI_BUS13_ANT0	AE25	DIO	BPI_ANT0	DVDD18
BPI_BUS14_ANT1	AE3	DIO	BPI_ANT1	DVDD18
BPI_BUS15_ANT2	AF24	DIO	BPI_ANT2	DVDD18
BPI_PA_VM0	AD3	DIO	PA_VM0	DVDD18
BPI_PA_VM1	AE2	DIO	PA_VM1	DVDD18
BPI_BUS11_OLAT0	AD4	DIO	BPI control	DVDD18
BPI_BUS12_OLAT1	AE24	DIO	BPI control	DVDD18
ANT_SEL0	K5	DIO	BPI control	DVDD18
ANT_SEL1	K6	DIO	BPI control	DVDD18
ANT_SEL2	K4	DIO	BPI control	DVDD18
BSI				
RFIC0_BSI_CK	AF22	DIO	RFIC0 BSI CLK	DVDD18
RFIC0_BSI_D0	AE20	DIO	RFIC0 BSI DATA0	DVDD18
RFIC0_BSI_D1	AF21	DIO	RFIC0 BSI DATA1	DVDD18
RFIC0_BSI_D2	AG22	DIO	RFIC0 BSI DATA2	DVDD18
RFIC0_BSI_EN	AE21	DIO	RFIC0 BSI CS	DVDD18
MISC_BSI_DO_0	AF7	DIO	MISC_BSI_DO_0	DVDD18
MISC_BSI_CK_0	AG7	DIO	MISC_BSI_CK_0	DVDD18
MISC_BSI_DO_1	AF6	DIO	MISC_BSI_DO_1	DVDD18
MISC_BSI_CK_1	AF5	DIO	MISC_BSI_CK_1	DVDD18
MISC_BSI_DO_2	AD6	DIO	MISC_BSI_DO_2	DVDD18
MISC_BSI_CK_2	AE6	DIO	MISC_BSI_CK_2	DVDD18
MISC_BSI_DO_3	AD5	DIO	MISC_BSI_DO_3	DVDD18
MISC_BSI_CK_3	AE5	DIO	MISC_BSI_CK_3	DVDD18
MSDC0				
MSDC0_CLK	D25	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	B25	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	C26	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	D24	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	A25	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	C24	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	A23	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	B23	DIO	MSDC0 data5 pin	DVDD18_MSDC0
MSDC0_DAT6	B24	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	A26	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	B26	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	C25	DIO	MSDC0 Reset pin	DVDD18_MSDC0
MSDC1				
MSDC1_CLK	W26	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	W27	DIO	MSDC1 command pin	DVDD28_MSDC1

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
MSDC1_DAT0	Y27	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	Y26	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	AA27	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	W25	DIO	MSDC1 data3 pin	DVDD28_MSDC1
EFUSE				
DVDD_VQPS	AD18	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI				
EMI0_DQ0	C13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ1	C15	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ2	C14	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ3	E15	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ4	B15	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ5	D15	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ6	E16	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ7	B17	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ8	A17	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ9	E18	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ10	F18	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ11	C18	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ12	D19	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ13	E19	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ14	C19	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ15	A19	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ16	D10	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ17	C11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ18	C10	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ19	D12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ20	B13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ21	B11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ22	B12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ23	E11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ24	D20	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ25	E20	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ26	E21	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ27	D21	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ28	B20	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ29	C22	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ30	C21	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ31	A21	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS0_C	E14	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS0_T	D14	DIO	DRAM interface	AVDDQ_EMI

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
EMI0_DQS1_C	D17	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS1_T	E17	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS2_C	E13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS2_T	F13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS3_C	E22	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS3_T	D22	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA0	B8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA1	B7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA2	C7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA3	D6	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA4	B5	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA5	D5	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA6	C5	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA7	E6	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA8	E5	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA9	A5	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS0_N	A9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS1_N	E8	DIO	DRAM interface	AVDDQ_EMI
EMI0_DM0	B16	DIO	DRAM interface	AVDDQ_EMI
EMI0_DM1	C17	DIO	DRAM interface	AVDDQ_EMI
EMI0_DM2	E10	DIO	DRAM interface	AVDDQ_EMI
EMI0_DM3	B19	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE0	D8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE1	E7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_C	E9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_T	F9	DIO	DRAM interface	AVDDQ_EMI
EMI_EXTR	B4	DIO	DRAM interface	AVDD2_EMI
VREF_EMI	F16	DIO	DRAM interface	AVDD2_EMI
AVDD18_DDR	H21	P	DRAM power	AVDD18_DDR
AVDD2_EMI	H10, ...	P	DRAM power	AVDD2_EMI
AVDDQ_EMI0	H11, ...	P	DRAM power	AVDDQ_EMI
AVDDQ_EMI1	H18, ...	P	DRAM power	AVDDQ_EMI
CAM				
CAM_CLK0	W5	DIO	Master clock to 1st sensor	DVDD18
CAM_CLK1	W2	DIO	Master clock to 2nd sensor	DVDD18
CAM_CLK2	J2	DIO	Master clock to 3rd sensor	DVDD18
CAM_CLK3	AG24	DIO	Master clock to 4th sensor	DVDD18
CAM_RST0	V2	DIO	Reset control to 1st sensor	DVDD18
CAM_RST1	V1	DIO	Reset control to 2nd sensor	DVDD18
CAM_RST2	K3	DIO	Reset control to 3rd sensor	DVDD18

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
CAM_RST3	AF23	DIO	Reset control to 4th sensor	DVDD18
CAM_PDN0	W6	DIO	Power down to 1st sensor	DVDD18
CAM_PDN1	Y2	DIO	Power down to 2nd sensor	DVDD18
CAM_PDN2	K2	DIO	Power down to 3rd sensor	DVDD18
CAM_PDN3	L24	DIO	Power down to 4th sensor	DVDD18
I2C				
SCL0	AB5	DIO	I2C0 clock	DVDD18
SCL1	AE1	DIO	I2C1 clock	DVDD18
SCL2	V4	DIO	I2C2 clock	DVDD18
SCL3	AC21	DIO	I2C3 clock	DVDD18
SCL4	U6	DIO	I2C4 clock	DVDD18
SCL5	AB23	DIO	I2C5 clock	DVDD18
SCL6	J3	DIO	I2C6 clock	DVDD18
SDA0	AC4	DIO	I2C0 data	DVDD18
SDA1	AF1	DIO	I2C1 data	DVDD18
SDA2	V3	DIO	I2C2 data	DVDD18
SDA3	AC22	DIO	I2C3 data	DVDD18
SDA4	V6	DIO	I2C4 data	DVDD18
SDA5	AC23	DIO	I2C5 data	DVDD18
SDA6	J4	DIO	I2C6 data	DVDD18
CONN				
CONN_TOP_CLK	J6	DIO	Connsys TOP 2-wire interface	DVDD18
CONN_TOP_DATA	K7	DIO	Connsys TOP 2-wire interface	DVDD18
CONN_HRST_B	G3	DIO	Connsys reset	DVDD18
CONN_WB_PTA	G2	DIO	Connsys WIFI/BT PTA	DVDD18
CONN_BT_CLK	J5	DIO	Connsys BT 2-wire interface	DVDD18
CONN_BT_DATA	K8	DIO	Connsys BT 2-wire interface	DVDD18
CONN_WF_CTRL0	H5	DIO	Connsys WIFI 3-wire interface	DVDD18
CONN_WF_CTRL1	H4	DIO	Connsys WIFI 3-wire interface	DVDD18
CONN_WF_CTRL2	H3	DIO	Connsys WIFI 3-wire interface	DVDD18
CONN_TOP_CLK	J6	DIO	Connsys TOP 2-wire interface	DVDD18
CONN_TOP_DATA	K7	DIO	Connsys TOP 2-wire interface	DVDD18
CONN_HRST_B	G3	DIO	Connsys reset	DVDD18
ABB				
REFP	AF18	AIO	ABB interface	AVDD18_AP
AUXIN0	AF20	AIO	ABB interface	AVDD18_AP
AUXIN1	AF19	AIO	ABB interface	AVDD18_AP
AUXIN2	AE19	AIO	ABB interface	AVDD18_AP
AUXIN3	AE18	AIO	ABB interface	AVDD18_AP
AUXIN4	AE17	AIO	ABB interface	AVDD18_AP
MAIN_X26M_IN	AB13	AIO	ABB interface	AVDD18_MD

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
PRX_BB_Q1	AG15	AIO	ABB interface	AVDD18_MD
PRX_BB_I1	AF15	AIO	ABB interface	AVDD18_MD
DRX_BB_Q1	AF16	AIO	ABB interface	AVDD18_MD
DRX_BB_I1	AG16	AIO	ABB interface	AVDD18_MD
DET_IN0	AF9	AIO	ABB interface	AVDD18_MD
DET_IP0	AG9	AIO	ABB interface	AVDD18_MD
DET_QP0	AF10	AIO	ABB interface	AVDD18_MD
DET_QN0	AG10	AIO	ABB interface	AVDD18_MD
TX_BB_QP0	AE10	AIO	ABB interface	AVDD18_MD
TX_BB_QN0	AD10	AIO	ABB interface	AVDD18_MD
TX_BB_IN0	AD9	AIO	ABB interface	AVDD18_MD
TX_BB_IP0	AE9	AIO	ABB interface	AVDD18_MD
PRX_BB_Q0P	AF12	AIO	ABB interface	AVDD18_MD
PRX_BB_Q0N	AG12	AIO	ABB interface	AVDD18_MD
PRX_BB_I0P	AF13	AIO	ABB interface	AVDD18_MD
PRX_BB_I0N	AG13	AIO	ABB interface	AVDD18_MD
DRX_BB_Q0P	AD12	AIO	ABB interface	AVDD18_MD
DRX_BB_Q0N	AE12	AIO	ABB interface	AVDD18_MD
DRX_BB_I0P	AD13	AIO	ABB interface	AVDD18_MD
DRX_BB_I0N	AE13	AIO	ABB interface	AVDD18_MD
RFIC_ET0_N	AC9	AIO	ABB interface	AVDD18_MD
RFIC_ET0_P	AD8	AIO	ABB interface	AVDD18_MD
APC	AC10	AIO	ABB interface	AVDD18_MD
MIPI				
DSI0_D3N	R27	AIO	DSI interface	AVDD12_DSI
DSI0_D3P	P27	AIO	DSI interface	AVDD12_DSI
DSI0_D1N	N27	AIO	DSI interface	AVDD12_DSI
DSI0_D1P	N28	AIO	DSI interface	AVDD12_DSI
DSI0_CKN	P26	AIO	DSI interface	AVDD12_DSI
DSI0_CKP	P25	AIO	DSI interface	AVDD12_DSI
DSI0_D0N	N26	AIO	DSI interface	AVDD12_DSI
DSI0_D0P	N25	AIO	DSI interface	AVDD12_DSI
DSI0_D2N	R26	AIO	DSI interface	AVDD12_DSI
DSI0_D2P	R25	AIO	DSI interface	AVDD12_DSI
CSI0A_L0P	N3	AO	CSI interface	AVDD12_CSI
CSI0A_L0N	N4	AIO	CSI interface	AVDD12_CSI
CSI0A_L1P	N1	AIO	CSI interface	AVDD12_CSI
CSI0A_L1N	N2	AIO	CSI interface	AVDD12_CSI
CSI0A_L2P	P1	AIO	CSI interface	AVDD12_CSI
CSI0A_L2N	P2	AIO	CSI interface	AVDD12_CSI
CSI0B_L0P	P3	AIO	CSI interface	AVDD12_CSI

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
CSI0B_L0N	P4	AIO	CSI interface	AVDD12_CSI
CSI0B_L1P	R3	AIO	CSI interface	AVDD12_CSI
CSI0B_L1N	R4	AIO	CSI interface	AVDD12_CSI
CSI0B_L2P	N5	AIO	CSI interface	AVDD12_CSI
CSI0B_L2N	P5	AIO	CSI interface	AVDD12_CSI
CSI1A_L0P	L3	AIO	CSI interface	AVDD12_CSI
CSI1A_L0N	L4	AIO	CSI interface	AVDD12_CSI
CSI1A_L1P	L1	AIO	CSI interface	AVDD12_CSI
CSI1A_L1N	L2	AIO	CSI interface	AVDD12_CSI
CSI1A_L2P	M1	AIO	CSI interface	AVDD12_CSI
CSI1A_L2N	M2	AIO	CSI interface	AVDD12_CSI
CSI1B_L0P	L5	AIO	CSI interface	AVDD12_CSI
CSI1B_L0N	M5	AIO	CSI interface	AVDD12_CSI
CSI1B_L1P	M3	AIO	CSI interface	AVDD12_CSI
CSI1B_L1N	M4	AIO	CSI interface	AVDD12_CSI
CSI2A_L0P	R1	AIO	CSI interface	AVDD12_CSI
CSI2A_L0N	R2	AIO	CSI interface	AVDD12_CSI
CSI2A_L1P	T1	AIO	CSI interface	AVDD12_CSI
CSI2A_L1N	T2	AIO	CSI interface	AVDD12_CSI
CSI2A_L2P	T3	AIO	CSI interface	AVDD12_CSI
CSI2A_L2N	T4	AIO	CSI interface	AVDD12_CSI
CSI2B_L0P	U3	AIO	CSI interface	AVDD12_CSI
CSI2B_L0N	U4	AIO	CSI interface	AVDD12_CSI
CSI2B_L1P	R5	AIO	CSI interface	AVDD12_CSI
CSI2B_L1N	T5	AIO	CSI interface	AVDD12_CSI
USB				
USB_DM	B27	AIO	USB D+ differential data line	AVDD33_USB
USB_DP	C27	AIO	USB D- differential data line	AVDD33_USB
CHD_DM	E26	AIO	BC1.1 charger DP	AVDD33_USB
CHD_DP	D26	AIO	BC1.1 charger DM	AVDD33_USB
WBG				
BT_QN	F3	AIO	BT Q channel negative-end	AVDD18_WBG
BT_QP	E3	AIO	BT Q channel positive-end	AVDD18_WBG
BT_IP	D2	AIO	BT I channel positive-end	AVDD18_WBG
BT_IN	D1	AIO	BT I channel negative-end	AVDD18_WBG
WF_QP	B1	AIO	Wifi Q channel positive-end	AVDD18_WBG
WF_QN	B2	AIO	Wifi Q channel negative-end	AVDD18_WBG
WF_IN	A2	AIO	Wifi I channel negative-end	AVDD18_WBG
WF_IP	A3	AIO	Wifi I channel positive-end	AVDD18_WBG
GPS_Q	G1	AIO	GPS Q channel	AVDD18_WBG
GPS_I	F1	AIO	GPS I channel	AVDD18_WBG

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
XIN_WBG	G7	AIO	WBG crystal clock input	AVDD18_WBG
MISC				
DRVBUS	AB26	DIO	This signal enables to drive 5V on Vbus. 0: Not drive Vbus 1: Drive 5V on Vbus	DVDD18
IDDIG	AB27	DIO	Indicates whether the connected plug is a mini-A or mini-B 0: Connected plug is a mini-A (ID is connected to GND). 1: Connected plug is a mini-B (ID is floating).	DVDD18
TN_PLLGP	W12	AIO	Reserved	-
TP_PLLGP	W13	AIO	Reserved	-
Analog Power				
AVDD04_DSI	T28	P	Analog power for DSI	-
AVDD12_MD	AG21	P	Analog power for modem	-
AVDD12_PLLGP	T14	P	Analog power for PLL	-
AVDD12_USB	E28	P	Analog power for USB	-
AVDD12_DSI	R28	P	Analog power for DSI	-
AVDD12_CSI	U2	P	Analog power for CSI	-
AVDD12_WBG	C3	P	Analog power for WBG	-
AVDD18_AP	AG18	P	Analog power input 1.8V	-
AVDD18_CPU	AC18	P	Analog power input 1.8V for CPU	-
AVDD18_MD	AG19	P	Analog power input 1.8V for modem	-
AVDD18_PLLGP	T16	P	Analog power input 1.8V for PLL	-
AVDD18_USB	D28	P	Analog power 1.8V for USB	-
AVDD18_WBG	H2	P	Analog power 1.8V for WBG (Wi-Fi, BT, GPS)	-
AVDD33_USB	B28	P	Analog power 3.3V for USB	-
Digital Power				
DVDD_DVFS	U16, ...	P	Digital power input for DVFS	-
DVDD_TOP	J21, ...	P	Digital power input for Vcore	-
DVDD_MFGSYS	K20, ...	P	Digital power input for GPU	-
DVDD_VDD_MODEM	R9, ...	P	Digital power input for LTE	-
DVDD_TOP_SRAM	L13, ...	P	Digital power input for SRAM	-
DVDD_MCUSYS_SRAM	V15	P	Digital power input for DVFS SRAM	-
DVDD_MFG_SRAM	R19	P	Digital power input for GPU SRAM	-
DVDD18_IOLT	G28	P	Digital power input for IO (region 1)	-
DVDD18_IOLM	W28	P	Digital power input for IO (region 2)	-
DVDD18_IOBL	AG27	P	Digital power input for IO (region 3)	-
DVDD18_IORB	U1, ...	P	Digital power input for IO (region 4)	-
DVDD18_IORT	J1	P	Digital power input for IO (region 5)	-
DVDD18_MSDC0	A27	P	Digital power input for MSDC0	-

© 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pin name	Pin no.	Type	Description	Power domain
DVDD18_MSDC1	AA28	P	Digital power input for MSDC1	-
DVDD28_MSDC1	AD28	P	Digital power input for MSDC1	-
DVDD18_SIM	AB28	P	Digital power input for SIM1/2	-
DVDD28_SIM1	AE28	P	Digital power input for SIM1	-
DVDD28_SIM2	AC28	P	Digital power input for SIM2	-
ESD				
CDM3P5A	AC5	G	Analog ground	-
CDM5P5A	AB6	G	Analog ground	-
Digital Ground				
DVSS	A11, ...	G	Ground input	-
Misc				
NC	A1, ...	-	Not connected	-

Table 2-4. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or pin name	Description	Max.	Unit
AVDD18_DDR AVDD18_PLLGP	Analog power input 1.8V for PLL & DDR	1.89	V
AVDD12_PLLGP	Analog power input 1.2V for PLL & DDR	1.26	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.89	V
AVDD12_MD	Analog power input 1.2V for BBTX, BBRX	1.26	V
AVDD12_CSI	Analog power input 1.2V for CSI	1.26	V
AVDD12_DSI	Analog power input 1.2V for DSI	1.26	V
AVDD04_DSI	Analog power input for DSI	0.88	V
AVDD33_USB	Analog power 3.3V for USB	3.22	V
AVDD18_USB	Analog power 1.8V for USB	1.89	V
AVDD12_USB	Analog power 1.2V for USB	1.26	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.89	V
AVDD12_WBG	Analog power 1.2V for connectivity ABB	1.26	V
DVDD18_IOLT DVDD18_IOLM DVDD18_SIM DVDD18_IOBL DVDD18_IORB DVDD18_IORT DVDD18_MSDC1	Digital power input for 1.8V IO	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1. 95	V
DVDD28_MSDC1	Digital power input for MSDC1	3.3	V
DVDD28_SIM1	Digital power input for SIM1	3.3	V
DVDD28_SIM2	Digital power input for SIM2	3.3	V
DVDD2 DVDDQ	Digital power input for DRAM	1.26	V
DVDD_DVFS_SRAM	Digital power input for SRAM	1.12	V
DVDD_DVFS	Digital power input for DVFS	1.076	V
DVDD_MFG_SRAM	Digital power input for SRAM	0.945	V
DVDD_MFG	Digital power input for GPU	0.945	V
DVDD_MODEM	Digital power input for MODEM	0.84	V
DVDD_TOP_SRAM	Digital power input for SRAM	0.945	V
DVDD_MD1	Digital power input for MD1	0.84	V
DVDD_TOP	Digital power input for TOP	0.84	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_DDR AVDD18_PLLGP	Analog power input 1.8V for PLL & DDR	1.71	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AUXADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD12_MD	Analog power input 1.2V for BBTX, BBRX	1.14	1.2	1.26	V
AVDD12_CSI	Analog power input 1.2V for CSI	1.14	1.2	1.26	V
AVDD12_DSI	Analog power input 1.2V for DSI	1.14	1.2	1.26	V
AVDD04_DSI	Analog power input for DSI	0.54	0.7	0.88	V
AVDD33_USB	Analog power 3.3V for USB	2.92	3.07	3.22	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD12_USB	Analog power 1.8V for USB	1.14	1.2	1.26	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
AVDD12_WBG	Analog power 1.2V for connectivity ABB	1.14	1.2	1.26	V
DVDD18_IOTL DVDD18_IOLM DVDD18_SIM DVDD18_IOBL DVDD18_IORB DVDD18_IORT DVDD18_MSDC1	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.7	1.8	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	1.8	1.9	V
		2.7	3.0	3.3	
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7	3	3.3	V
		1.68	1.8	1.92	
DVDD2 DVDDQ	Digital power input for EMI (LPDDR3)	1.14	1.2	1.26	V
DVDD2	Digital power input for EMI (LPDDR4X)	1.06	1.1	1.17	V
DVDDQ	Digital power input for EMI (LPDDR4X)	0.57	0.6	0.65	V
DVDD_DVFS_SRAM	Digital power input for CPU SRAM	0.85	-	1.12	V
DVDD_DVFS	Digital power input for CPU (0.55V is only for idle state)	0.5225	0.55	0.5775	V
		0.6175	0.65	0.6825	
		0.665	0.7	0.735	
		0.76	0.8	0.84	
		0.855	0.9	0.945	
		0.972	1.023	1.074	
DVDD_MFG_SRAM	Digitla power input for GPU SRAM	0.855	0.9	0.945	V
DVDD_MFG	Digital power input for GPU	0.76	0.8	0.84	V
		0.665	0.7	0.735	
		0.617	0.65	0.682	
DVDD_MD1	Digital power input for MD1	0.76	0.8	0.84	V

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
		0.665	0.7	0.735	
DVDD_MODEM	Digital power input for MODEM	0.76	0.8	0.84	V
		0.665	0.7	0.735	
DVDD_TOP_SRAM	Digital power input for TOP SRAM	0.855	0.9	0.945	V
DVDD_TOP	Digital power input for TOP	0.76	0.8	0.84	V
		0.665	0.7	0.735	
		0.618	0.65	0.683	

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
FRTC	Input clock frequency		32		kHz
DCRTC	Input signal duty cycle	45	50	55	%

2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2.4.3 I2C0, I2C1, I2C2 DC Electrical Characteristics

Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.3		2.0	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125* DVDD28_MSDC1	V

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V)

Parameters	Descriptions	Min	Typ	Max	Unit
VIH	Input logic low voltage	1.27		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

2.2.4.7 SIM DC Electrical Characteristics

Table 2-14. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR3

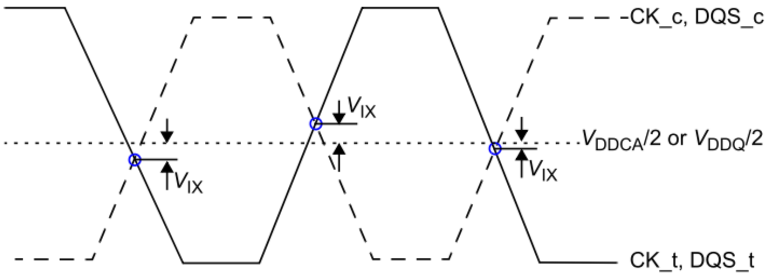


Figure 2-2. LPDDR3 VIX definition

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

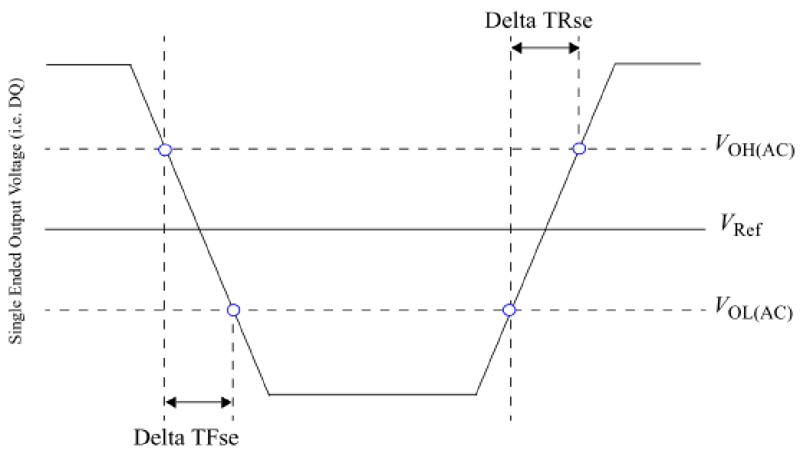


Figure 2-3. LPDDR3 single-ended output slew-rate definition

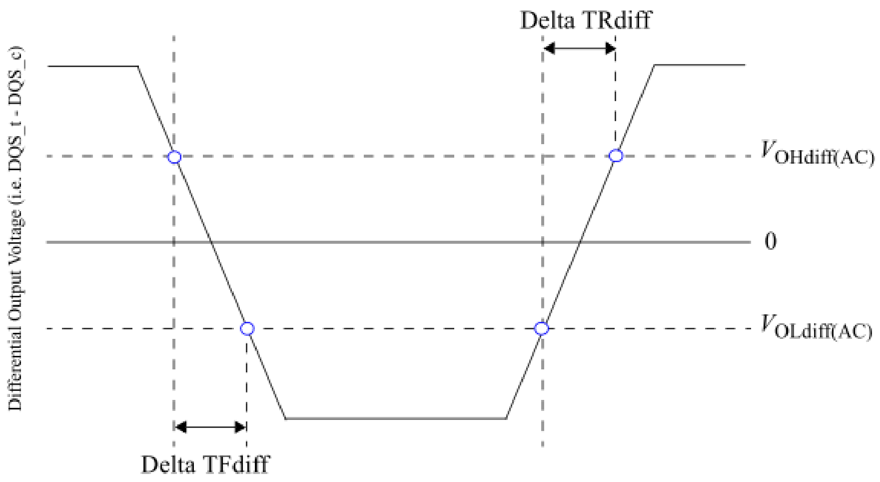


Figure 2-4. LPDDR3 differential output slew-rate definition

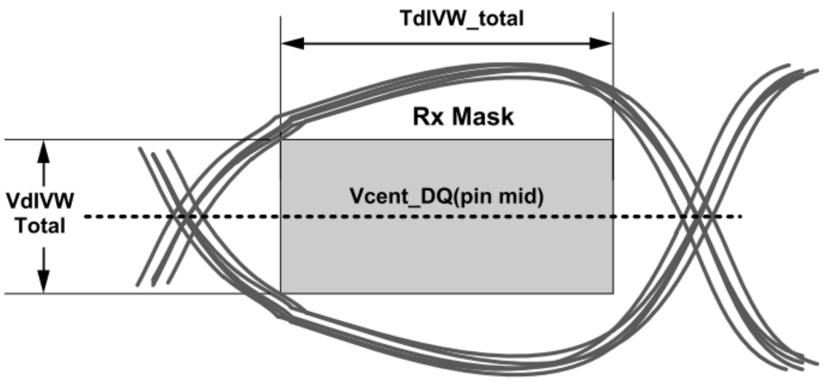


Figure 2-5. LPDDR3 RX mask

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 2-15. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
VIXCA	Differential input cross point voltage relative to VDDCA/2 for CK_t, CK_c	-120		120	mV
VIXDQ	Differential input cross point voltage relative to VDDQ/2 for DQS_t, DQS_c	-120		120	mV
SRQse	Single-ended output slew rate (RON = 40Ω +/- 30%)	1.5		4	V/ns
SRQdiff	Differential output slew rate (RON = 40Ω +/- 30%)	3		8	V/ns
VdIVW_total	Rx mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

2.2.5.2 External Memory Interface for LPDDR4X

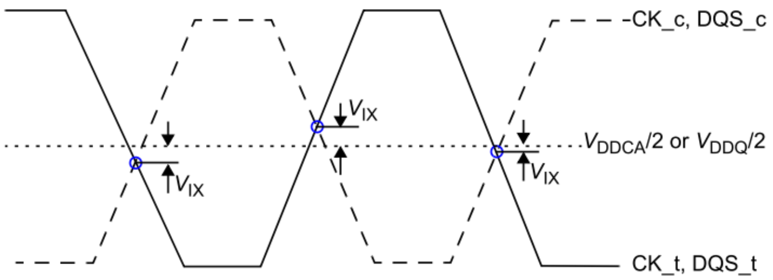


Figure 2-6. LPDDR4X VIX definition

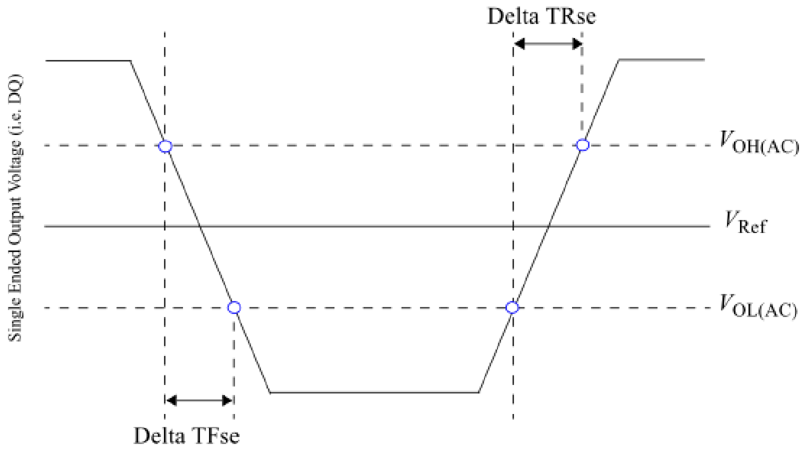


Figure 2-7. LPDDR4X single-ended output slew-rate definition

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

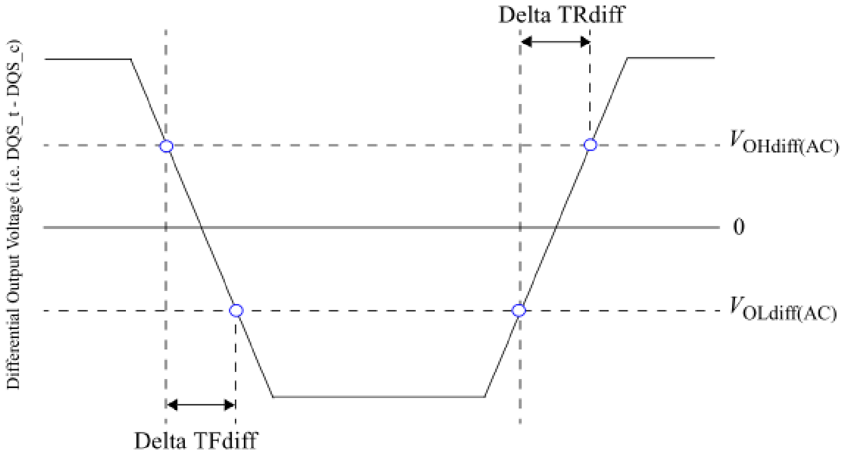


Figure 2-8. LPDDR4X differential output slew-rate definition

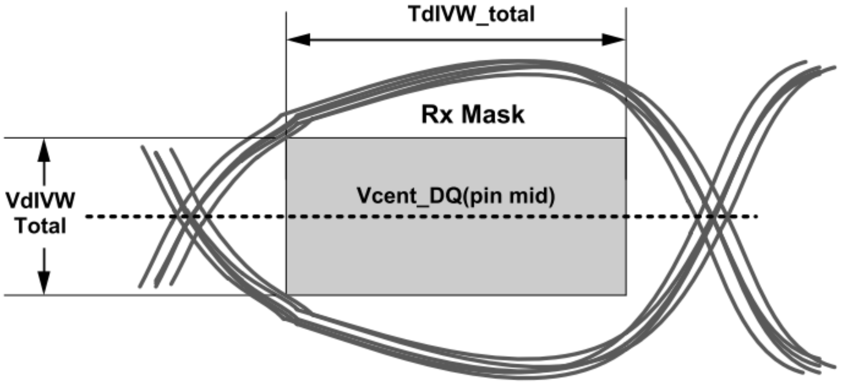


Figure 2-9. LPDDR4X RX mask

Table 2-16. LPDDR4X AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
Vix_DQS_ratio	DQS differential input crosspoint voltage ratio			20	%
Vix_CK_ratio	CK differential input crosspoint voltage ratio			25	%
SRQse (LPDDR4X)	Single-ended output slew rate	3		9	V/ns
SRQdiff (LPDDR4X)	Differential output slew rate	6		18	V/ns
VdIVW_total	Rx Mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2.5.3 SPI AC Timing Characteristics

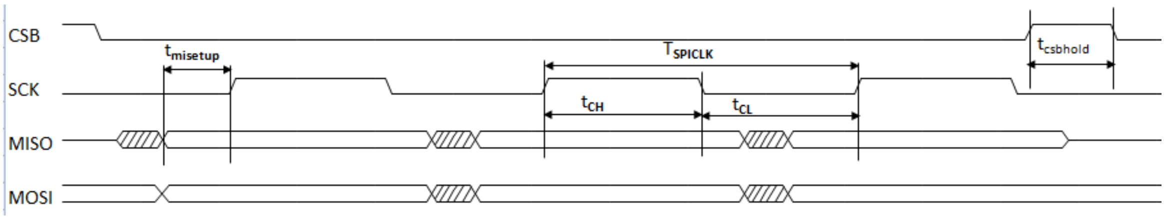


Figure 2-10. SPI timing diagram

Table 2-17. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	36.5	-	-	ns
SPI clock low time	t_{CL}	9.1	-	-	ns
SPI clock high time	t_{CH}	9.1	-	-	ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

2.2.5.4 I2S AC Timing Characteristics

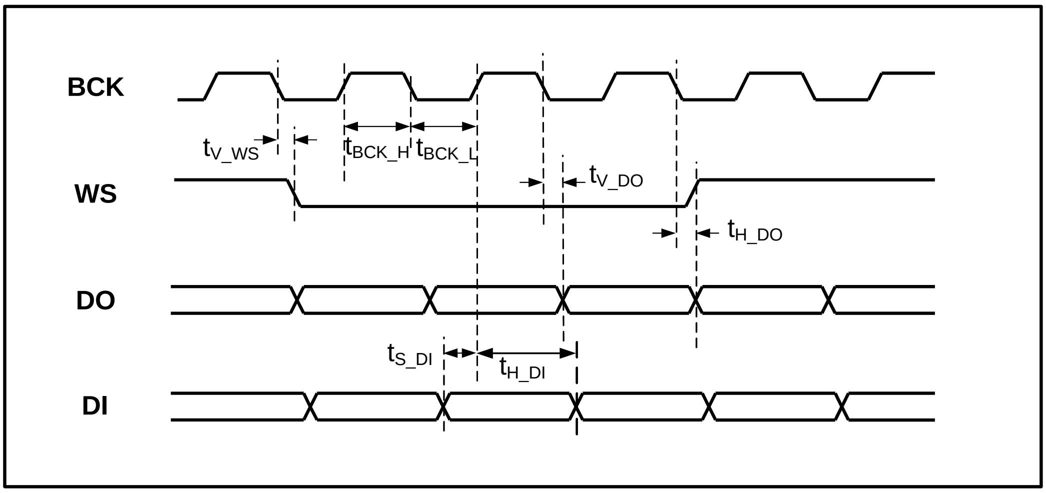


Figure 2-11. I2S master mode timing diagram

Table 2-18. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz
f_{BCK}	Serial clock frequency	32 * f_S	-	64 * f_S	MHz

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Description	Min.	Typ.	Max.	Unit
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

2.2.5.5 I2C AC Timing Characteristics

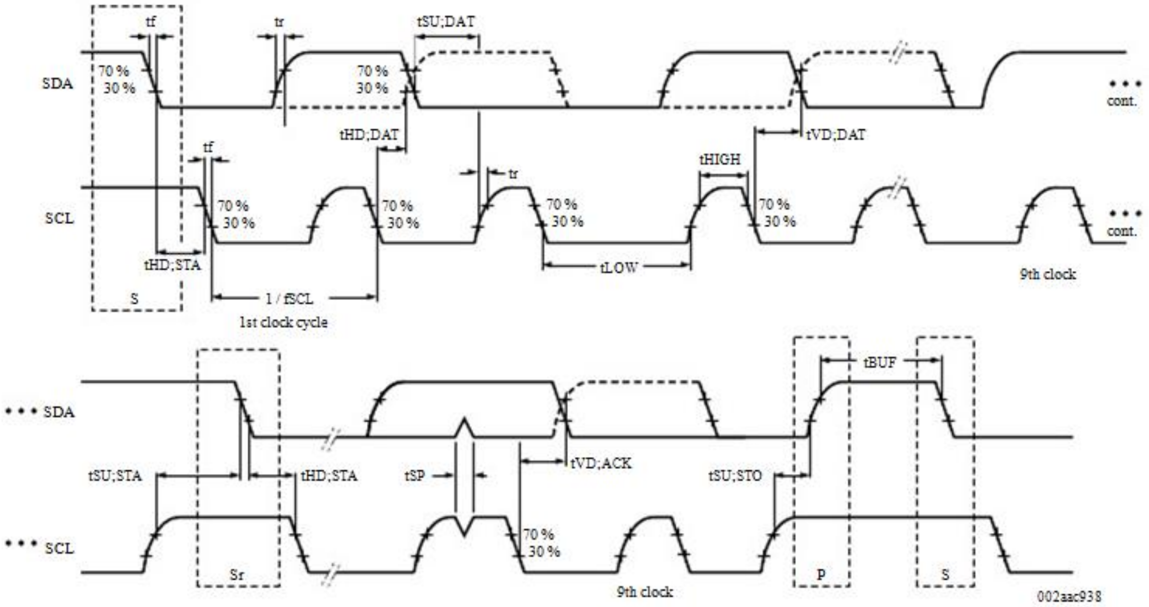


Figure 2-12. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-19. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2.5.6 MSDC AC Timing Characteristics

2.2.5.6.1 Default Speed Timing

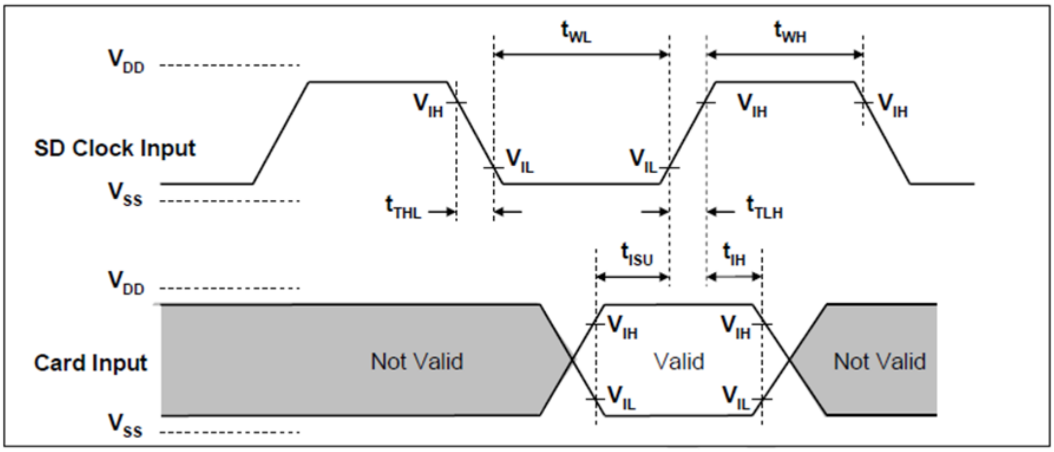


Figure 2-13. MSDC input timing diagram of default speed

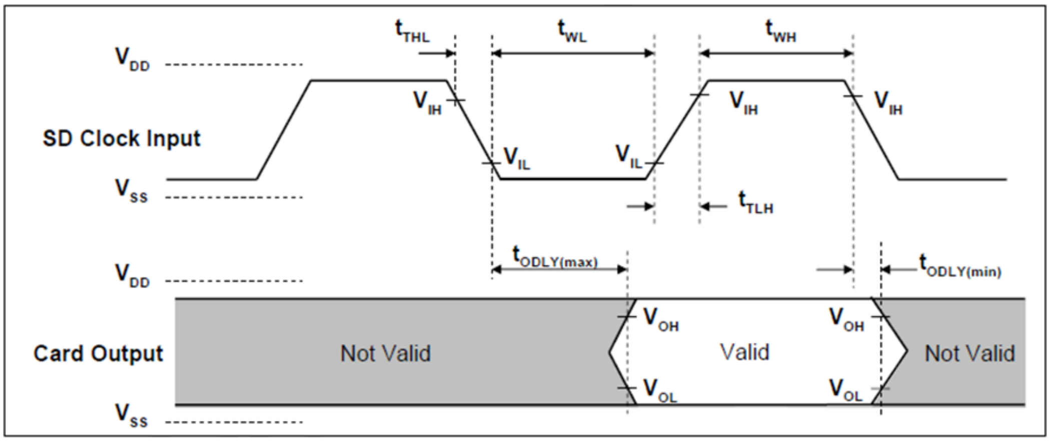


Figure 2-14. MSDC output timing diagram of default speed

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 2-20. MSDC AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD}≦10pF (1 card)
Clock frequency identification mode	f_{OD}	0(1) / 100	400	kHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD}≦10pF (1 card)
Input hold time	T_{IH}	5		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L≦40pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L≦40pF (1 card)

2.2.5.6.2 High Speed Timing

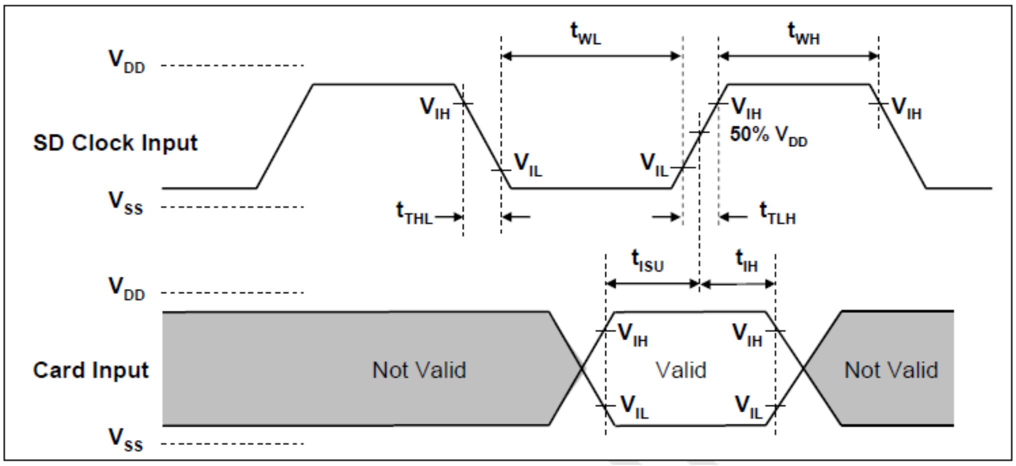


Figure 2-15. MSDC input timing diagram of high speed

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

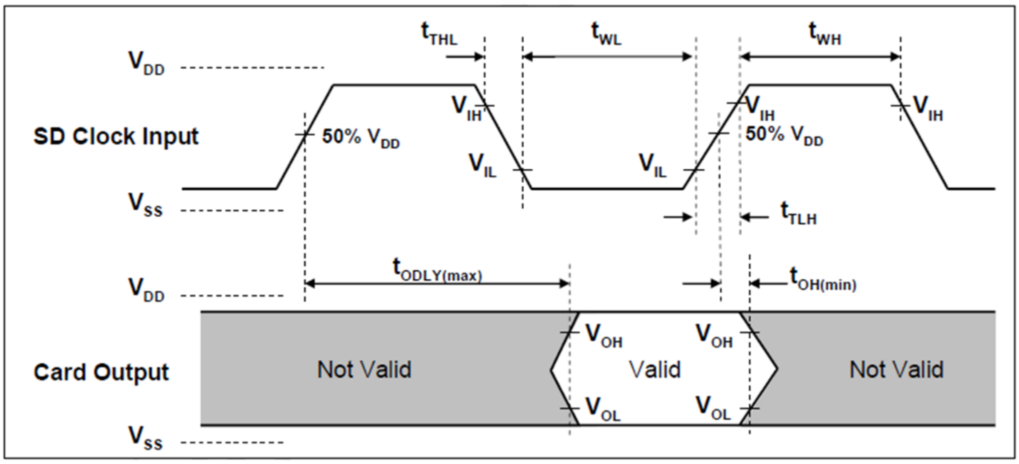


Figure 2-16. MSDC output timing diagram of high speed

Table 2-21. MSDC AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	C_L≦40pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L≧15pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.6.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

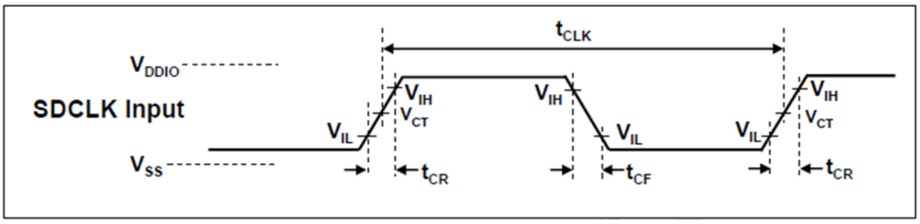


Figure 2-17. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

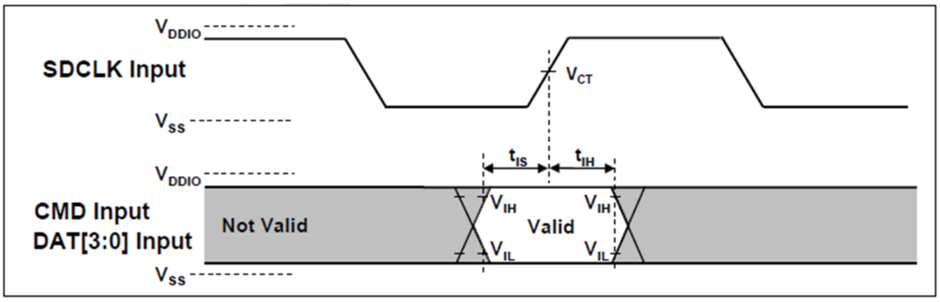


Figure 2-18. MSDC input timing diagram of SDR50/SDR104 mode

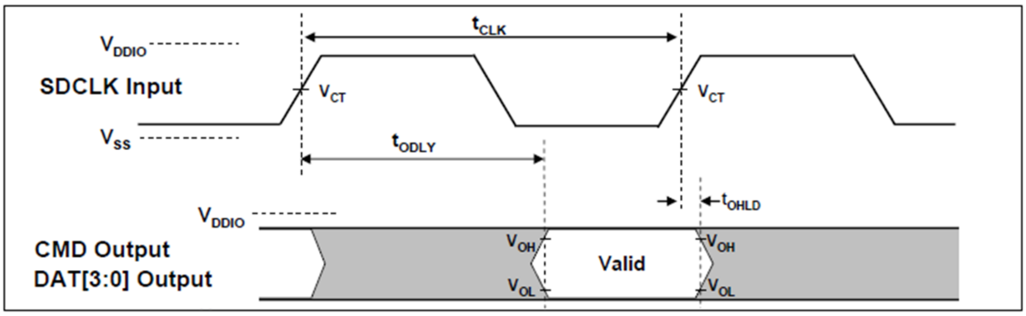


Figure 2-19. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50)

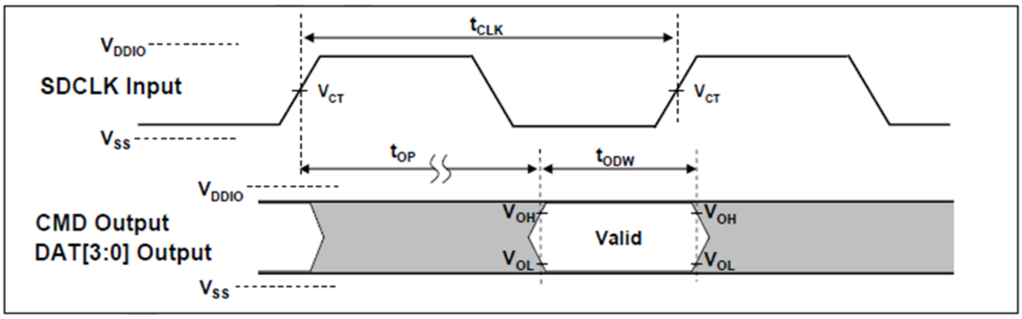


Figure 2-20. MSDC output timing diagram of variable window (SDR104)

Table 2-22. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (max.), between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute max. value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Symbol	Min.	Max.	Unit	Remark
Clock Duty	30	70	%	
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	t_{CLK}≧10.0ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	t_{CLK}≧20.0ns, C_L=40pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.6.4 DDR50 Speed Mode Timing

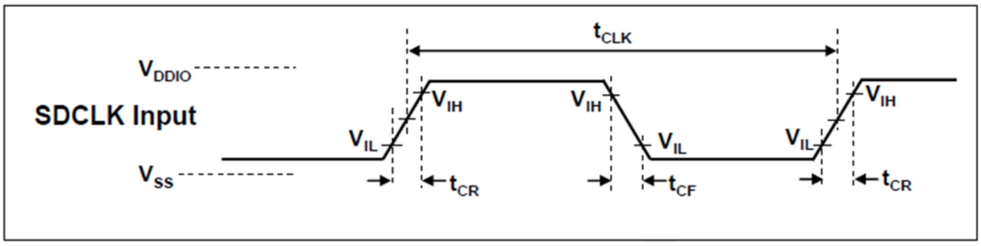


Figure 2-21. MSDC clock timing diagram of DDR50 speed mode

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

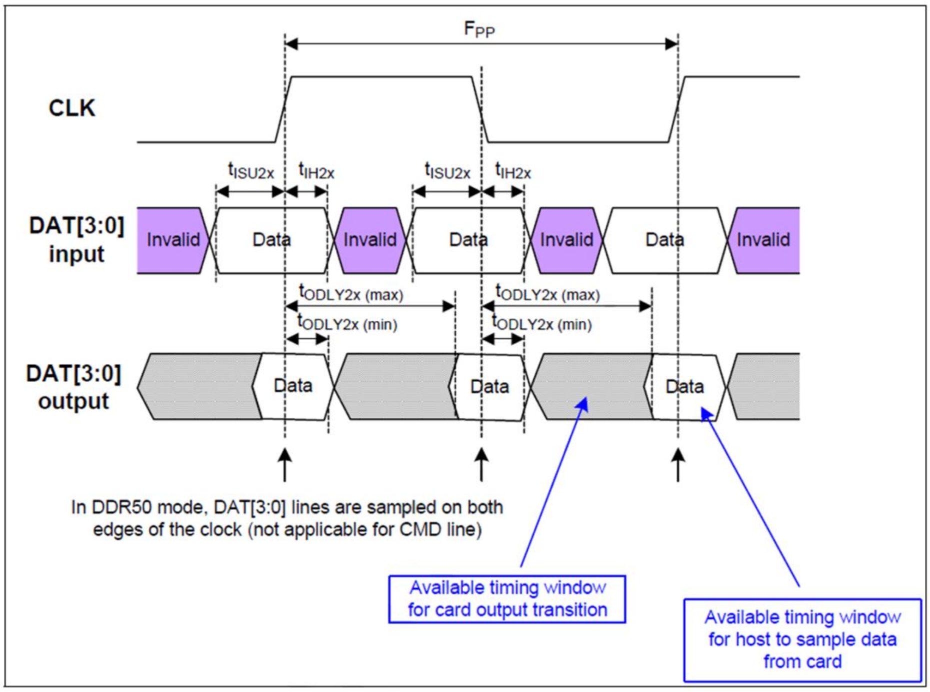


Figure 2-22. MSDC input/output timing diagram of DDR50 speed mode

Table 2-23. MSDC AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	C_L≦30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≧15pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	C_L≦25pF (1 card)
Output hold time	t_{OH}	1.5	-	Ns	C_L≧15pF (1 card)

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2.5.6.5 HS200 Speed Timing

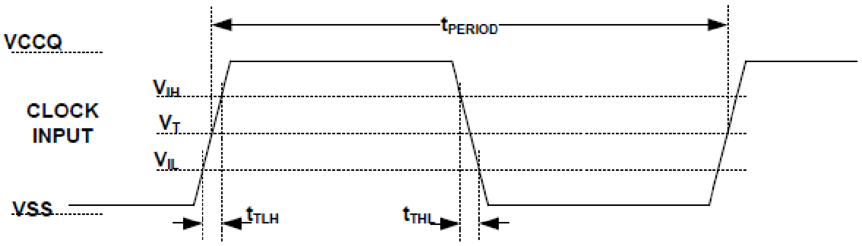
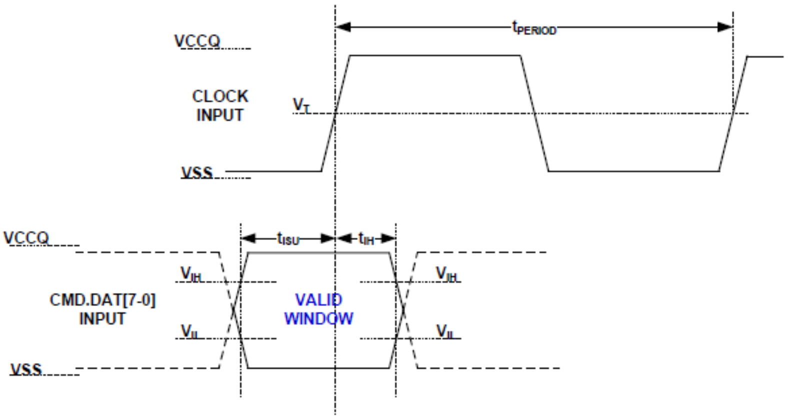


Figure 2-23. MSDC clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-24. MSDC input timing diagram of HS200

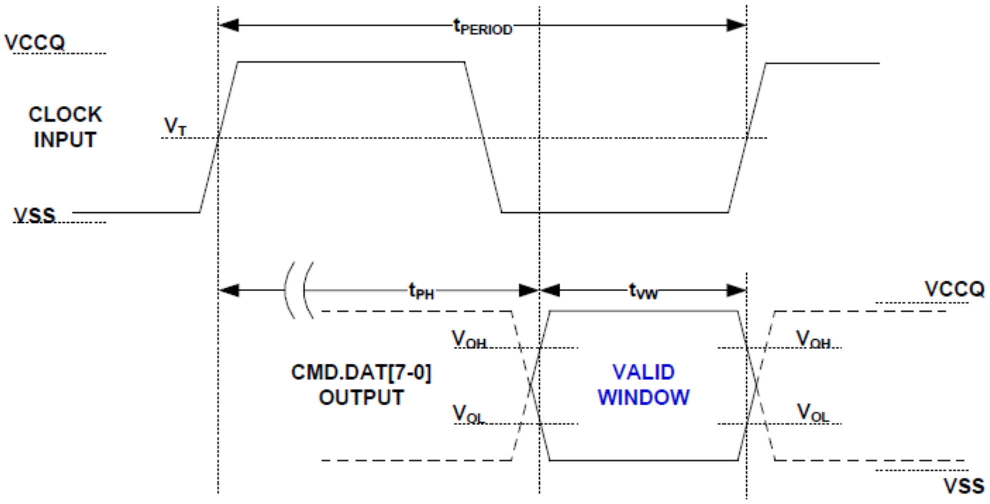


Figure 2-25. MSDC output timing diagram of HS200

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 2-24. MSDC AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (max.), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leqq$ 6pF
t_{IH}	0.80		ns	$C_{DEVICE} \leqq$ 6pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay varioation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

2.2.5.6.6 HS400 Speed Timing

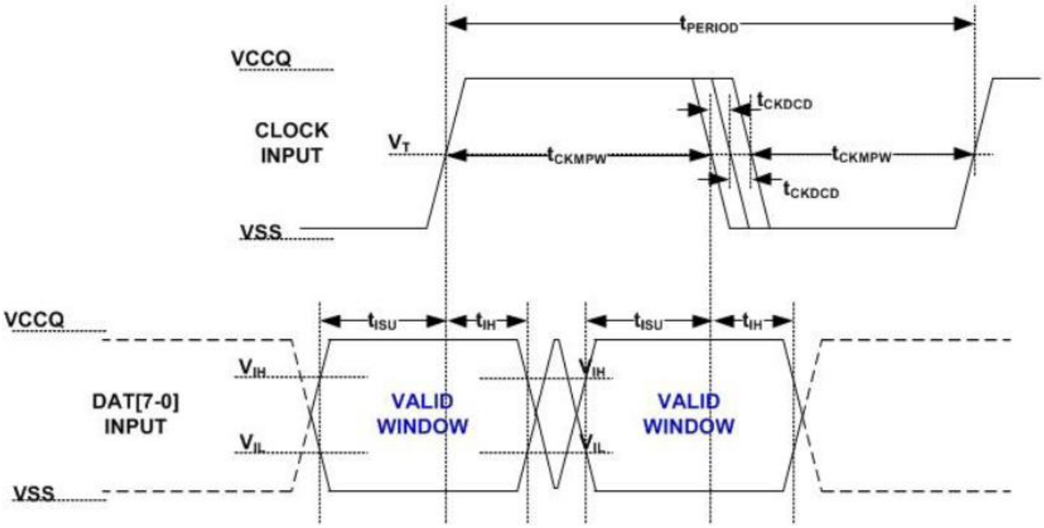


Figure 2-26. MSDC input timing diagram of HS400

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

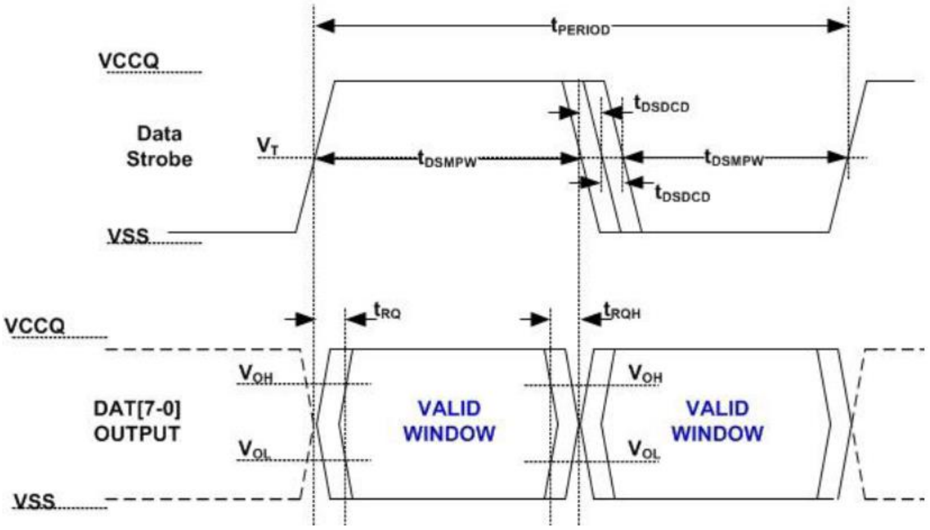


Figure 2-27. MSDC output timing diagram of HS400

Table 2-25. MSDC AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leqq 6$pF. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leqq 6$pF. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to Data Strobe)					

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Symbol	Min.	Max.	Unit	Remark
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.7 SIM AC Timing Characteristics

Table 2-26. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.3 System Configuration

2.3.1 Mode Selection

Table 2-27. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI0 [1] PWRAP_SPI0_CSN	00: Use SPI pin for legacy JTAG, DPI pin for IO_JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG (default) 11: Use SPI pin for legacy JTAG
[0] AUD_DAT_MISO0	0: NA (default) 1: USB DP/DM output JTAG
[0] AUD_DAT_MISO1	0: eMMC booting (default) 1: Reserved
[0] PWRAP_SPI0_MO [1] PWRAP_SPI0_MI	00: LPDDR3 01: Reserved 10: LPDDR4X 11: Reserved

2.3.2 Constant Tie Pins

Table 2-28. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.4 Power-on Sequence

The power-on/off sequence is shown in the following figure:

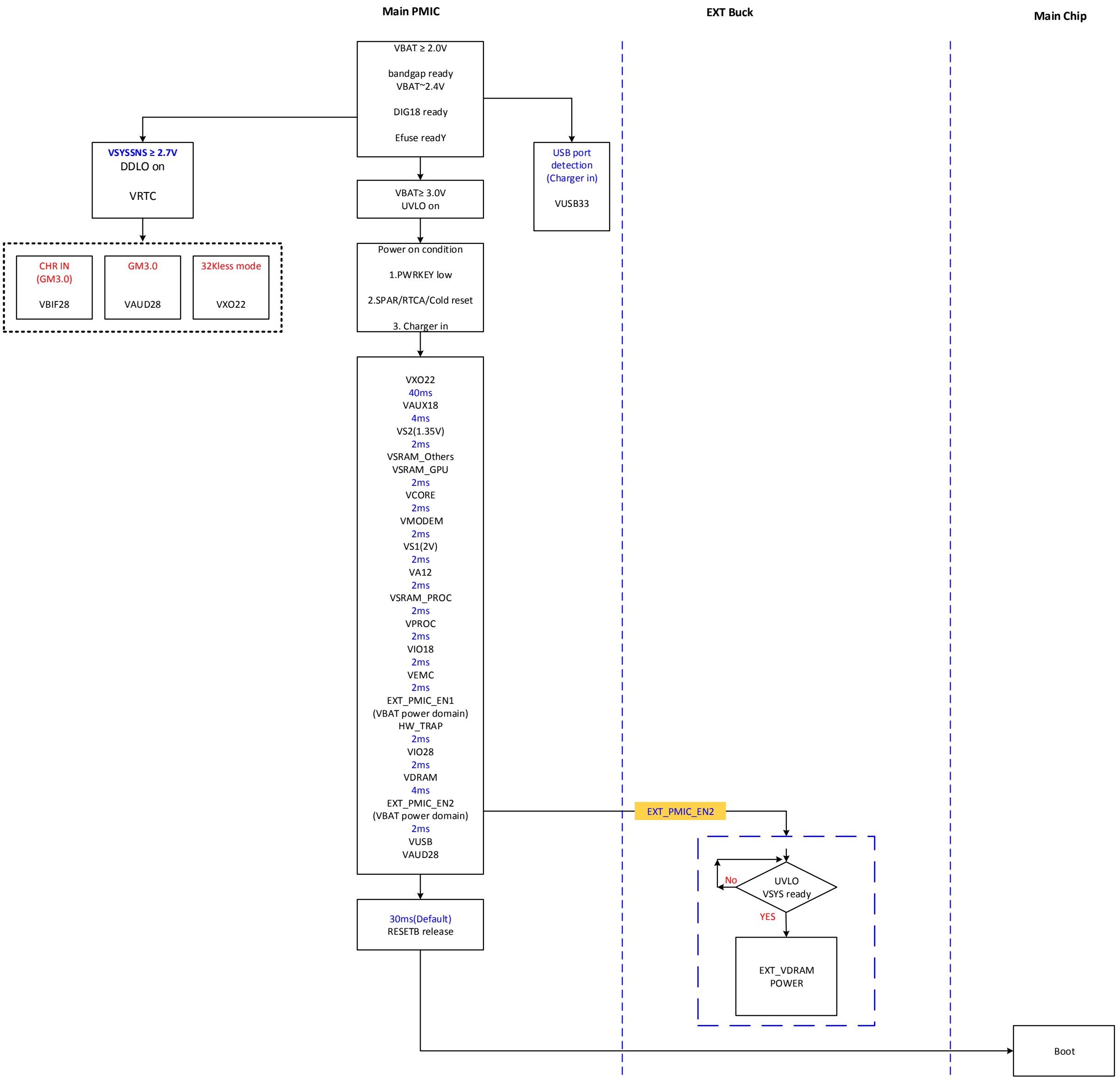


Figure 2-28. Power on sequence

Refer to PMIC datasheet for detailed timing sequence.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- DETADC: A ADC that detects calibration, thermal data from RF chip.
- RF control: A DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers.
- Auxiliary ADC: Provides an ADC for auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Clock Squarer
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1. Analog input multiplexer: For each channel, a multiplexer is included.
2. A/D converter: 8 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.
3. The first ADC set (PIQ1, DIQ1) supports both single-ended and differential input while the second ADC set (PIQ2, DIQ2) supports only single-ended input.

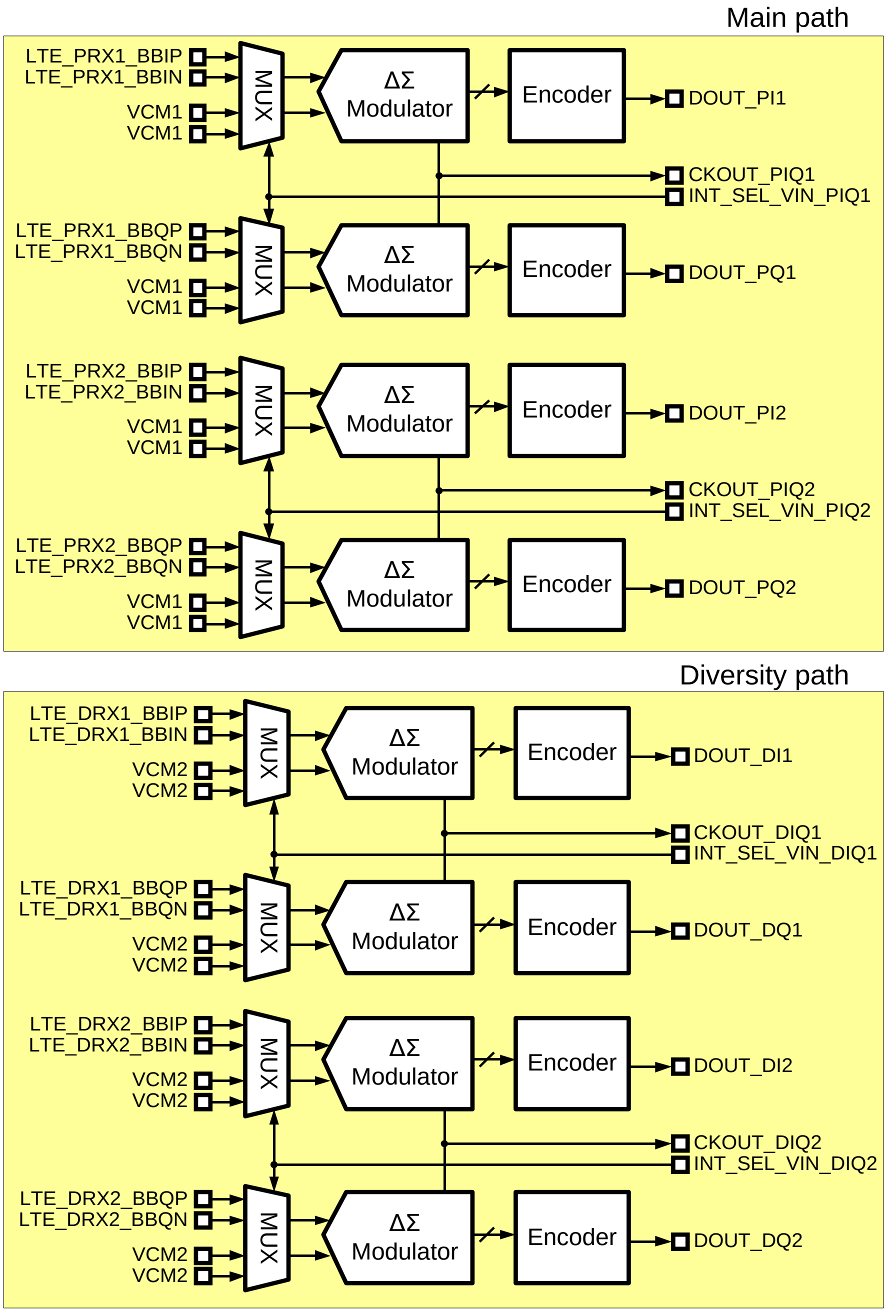


Figure 2-29. Block diagram of BBRX-ADC

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-29. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage Single-ended analog input			2.4 1.2	Vpp
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency	208		416	MHz
	Input clock duty cycle	49.5	50	50.5	%
RIN	Differential input resistance	2.8		20.8	kΩ
FS	Output sampling rate	208		416	MSPS
SIN	Signal to in-band noise	69		85	dB
AVDD	Analog power supply	1.7 1.1	1.8 1.2	1.9 1.3	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel, I_{BAT}) − Power-up − Power-down		2.7 10		mA uA

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 15 bits of thermometer code and 7 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

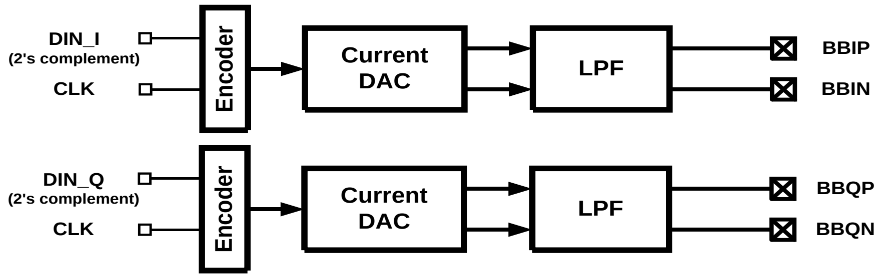


Figure 2-30. Block diagram of BBTX

2.5.3.2.2 Functional Specifications

Table 2-30. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40/80		MHz
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 8 10		 mA uA

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40/80MHz 1st-order Butterworth frequency response.

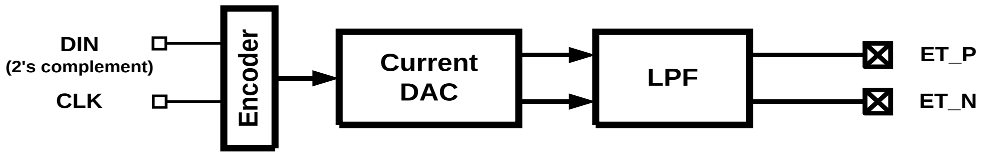


Figure 2-31. Block diagram of ETDAC

2.5.3.3.2 Functional Specfications

Table 2-31. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.615	0.65	0.685	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.
2. 12-bit A/D converters: Converts the detected signals to 12-bit digital data sampled at 208MHz.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

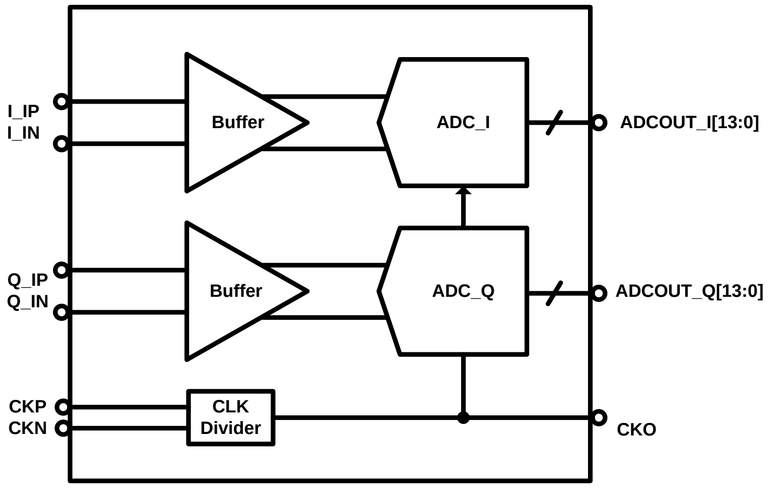


Figure 2-32. Block diagram of DETADC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

Table 2-32. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
FS	Sampling rate		208		MSPS
VOS	Differential input referred offset		30		mV
DR	Dynamic range		55		dB
IM3	3rd order Inter Modulation Distortion		-66		dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 6 1		 mA uA

 © 2018 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

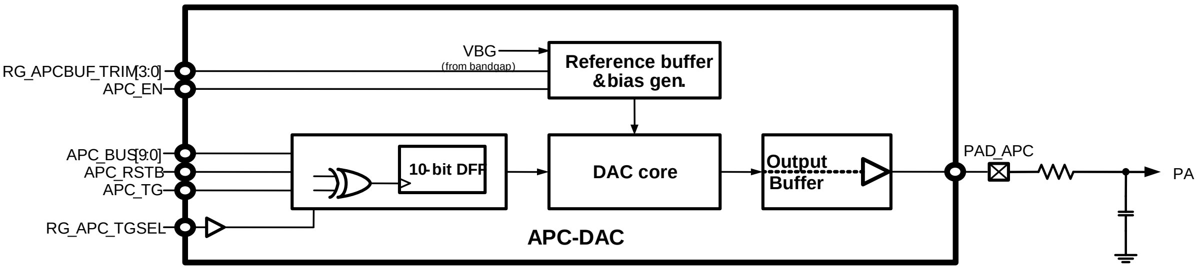


Figure 2-33. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-33. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	1000	pF
R_L	Output loading resistance		7		KΩ
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
AVDD	Analog power supply	1.71	1.8	1.89	V
T	Operating temperature	–20		85	°C
	Current consumption – Power-up – Power-down		 450 20		 uA uA

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-34. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		4/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel (PAD loading excluded)		 50 4		 fF pF
	Clock latency		N+8		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 2-35. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
	Maximum Positive Overshoot			1.98	V
	Minimum Negative Overshoot	-0.1			V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		650		uA

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-36. Temperature sensor specifications

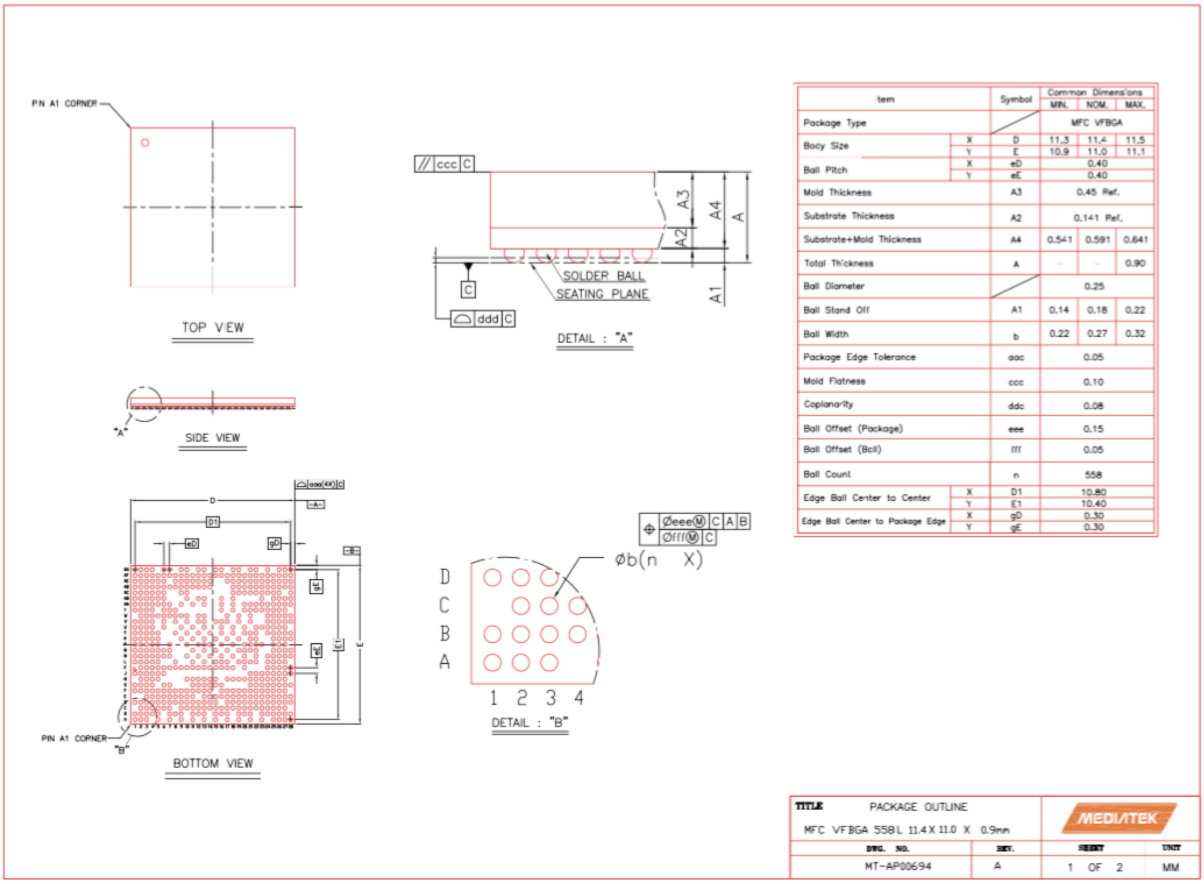
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	11.3	11.4	11.5
	Y	E	10.9	11.0	11.1
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.141 Ref.		
Substrate+Mold Thickness		A4	0.541	0.591	0.641
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.14	0.18	0.22
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aac	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddc	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	558		
Edge Ball Center to Center	X	D1	10.80		
	Y	E1	10.40		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

*Figure 2-34. Outlines and dimensions of VFBGA 11.4mm*11mm, 558-ball, 0.4mm pitch package*

2.6.2 Thermal Operating Specifications

Table 2-37. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	31.04	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.7 Power Delivery Network

Table 2-38. PDN specifications

Power Domain	RDC	RRemote	Frequency range: 0.1~100MHz, equivalent RLC model		
	(mΩ)	(mΩ)	R (mohm)	L (nH)	C (uF)
VPROC	12	1.5	12	0.15	28.5
VMODEM	25.4	3.2	25	0.30	41.0
VGPU	12.0	3.0	25	0.30	44.8
VMD1	12.0	12.9	25	0.30	
VCORE	12.0	3.6	25	0.20	
VEMI_VDD2	40	4	20	0.30	34.2
VEMI_VDDQ	150	15	20	0.30	
VDRAM_VDD2	40	4	20	0.30	
VDRAM_VDDQ	50	5	20	0.30	

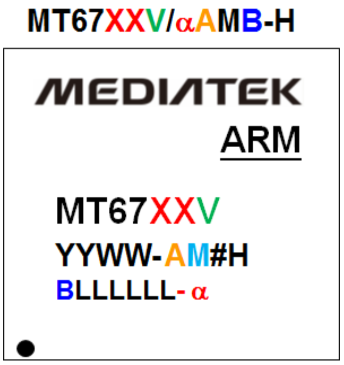
Note: Refer to document "MT6761_PDN_Checking_Notice.pdf" on DCC for more design concepts.

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.8 Ordering Information

2.8.1 Top Marking Definition



- MT No: 6761
- V: Package code
- YYWW: Date code
- #: Subcontractor code
- LLLLLLL: Lot number
- α: Function code

Figure 2-35. Top marking of MT6761

© 2018 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.